DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

***COURSE*: LINEAR IC APPLICATIONS**

***BRANCH**: Eletronics and communication Engineering*

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LECTURE NOTES

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INDEX

UNIT I

INTEGRATED CIRCUITS

INTEGRATED CIRCUITS

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits

1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

Depending upon the number of active devices per chip,there are different levels of integration

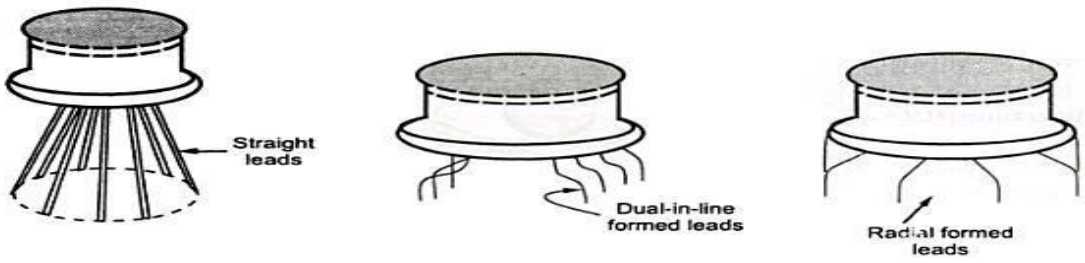
	Level of Integration	Number of active devices per chip
1.	Small scale integration (SSI)	Less than 100
2.	Medium scale integration (MSI)	100 - 10000
3.	Large scale integration (LSI)	1000 - 100,000
4.	Very large scale integration (VLSI)	Over 100,000
5.	Ultra large scale integration (ULSI)	Over 1 million

IC Package Types

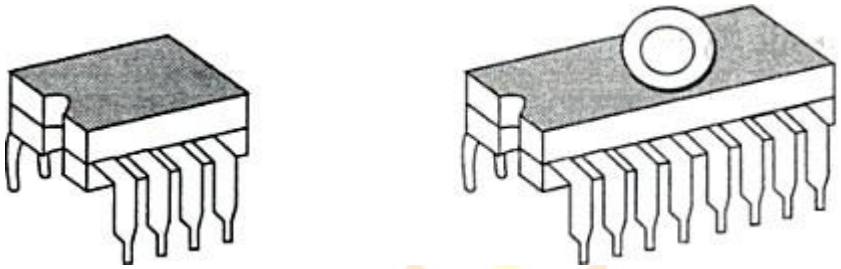
The op-amp ICs are available in various packages. The IC packages are classified as,

1. Metal Can
2. Dual In Line
3. Flat Pack

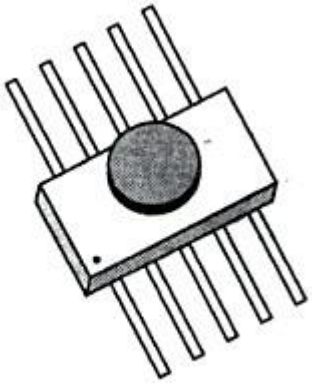
Metal Can package:



Dual- in- Line Package:



Flat Pack:



10 lead version

DIFFERENTIAL AMPLIFIER:

The differential amplifier consists of two symmetrical common-emitter sections and is capable of amplifying the difference between two input signals. The differential amplifier can amplify ac as well as dc input signals because it employs direct coupling.

There are four types of differential amplifier configurations:

(a) The dual Input, Balanced output differential amplifier

DC Analysis------ $I_E = V_{EE} - V_{BE}/2R_E$,

$V_{CE} = Vcc + V_{BE} - R_c I_c$

AC Analysis------- $A_d = R_C/r_e$

$R_{i1} = R_{i2} = 2\beta_{ac} r_e$

$R_{01} = R_{02} = R_c$

(b) The dual input, unbalanced output differential Amplifier

DC Analysis--------- $I_E = V_{EE} - V_{BE}/(2R_E + R_{in}/\beta_{dc})$

$V_{CE} = Vcc + V_{BE} - R_c I_{CQ}$

AC Analysis---------- $A_d=R_C/2r_e$

$R_{i1}= R_{i2}=2\beta_{ac}r_e$

$R_0= R_c$

(c) The single input, balanced output differential Amplifier

DC Analysis--------- $I_E =V_{EE} - V_{BE}/(2R_E+R_{in}/\beta_{dc})$

$V_{CE}=Vcc+ V_{BE}-R_cI_{CQ}$

AC Analysis---------- $I_E =V_{EE} - V_{BE}/(2R_E+R_{in}/\beta_{dc})$

$R_i=2\beta_{ac}r_e$

$R_{01}=R_{02}=R_c$

(d) The single input, unbalanced output differential Amplifier

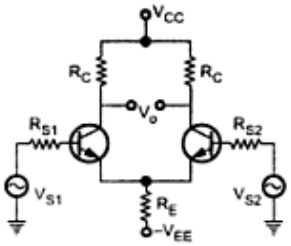
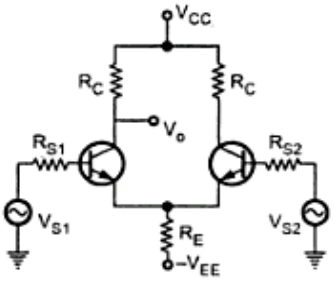
DC Analysis--------- $I_E =V_{EE} - V_{BE}/(2R_E+R_{in}/\beta_{dc})$

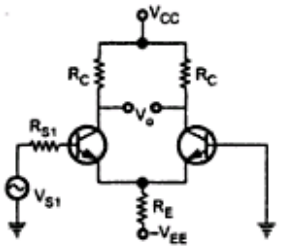
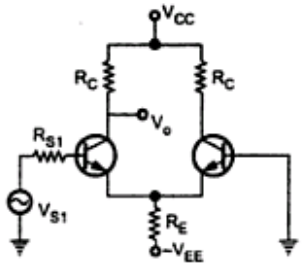
$V_{CE}=Vcc+ V_{BE}-R_cI_{CQ}$

AC Analysis --------- $A_d=R_C/2r_e$

$R_{i=}2\beta_{ac}r_e$

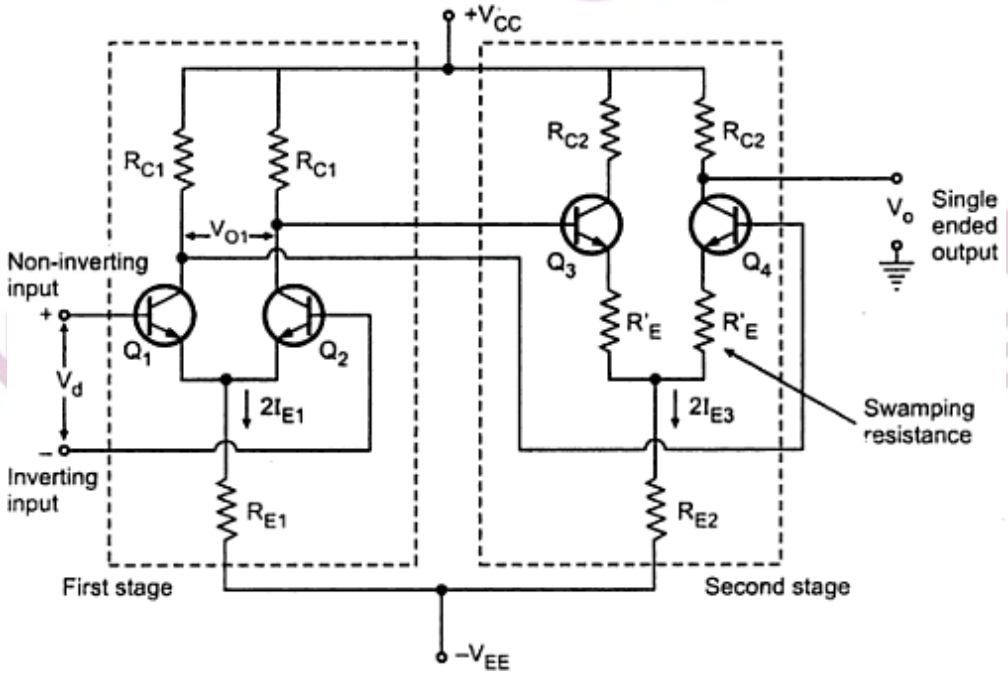
$R_0=$ R_c

Configuration	Circuit	A_d voltage gain	R_{in} Input Resistance	R_o Output Resistance
Dual Input Balanced Output		$\frac{h_{fe}\,R_C}{R_S + h_{ie}}$	$2(R_S + h_{ic})$	R_C
Dual Input Unbalanced Output		$\frac{h_{fe}\,R_C}{2(R_S + h_{ie})}$	$2(R_S + h_{ic})$	R_C

Single Input Balanced Output		$\frac{h_{fe} R_C}{R_S + h_{ie}}$	$2(R_S + h_{ic})$	R_C
Single Input Unbalanced Output		$\frac{h_{fe} R_C}{2(R_S + h_{ie})}$	$2(R_S + h_{ic})$	R_C

Cascade Differential Amplifier Stages:

In cascaded differential amplifier, the output of the first stage is used as an input for the second stage, the output of the second stage is applied as an input to the third stage, and so on. Because of direct coupling between the stages, the operating point of succeeding stages changes



The 741C Op Amp is connected in Inverting mode having following parameters Given: V_{in} = 0.6V, R_F = 20 KΩ , R_1 = 2 KΩ , A_{OL} = 400k , R_{in} = 8 MΩ , R_o = 60 Ω

Find : V_o , i_F , A_v , β , R_{inF} and R_{oF}

Solution:

$V_o = \left(-\frac{R_f}{R_1}\right) V_{in} = \left(-\frac{20}{2}\right) \times 0.6 = -6$ **Volt**

$I_F = \frac{V_{in}}{R_1} = \frac{0.6}{2000} =$ **0.3 mA**

(Also, $I_f = \frac{V_o - V_f}{R_f} = \frac{6-0}{20000} = \frac{6}{20000} =$ **0.3 mA)** *as V_F is virtual ground*

$A_v = \left(-\frac{R_f}{R_1}\right) = \left(-\frac{20}{2}\right) =$ **10**

$\beta = \frac{R_1}{R_1 + R_f} = \frac{2}{2+20} =$ **0.0909**

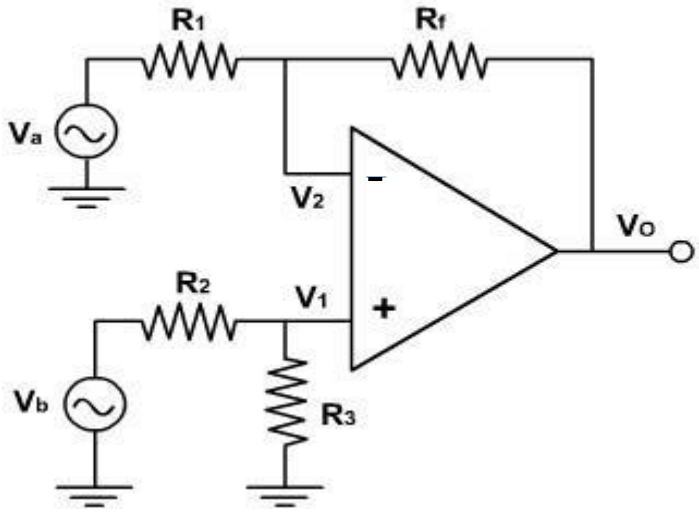
$R_{inF} = R_1 =$ **2000 Ω**

$R_{oF} = \frac{R_o}{1+\beta A_{oL}}$

Draw the circuit of differential amplifier using one Op. Amp. and derive the equation of differential gain (A_D).

The *differential amplifiers* amplify the difference between two input voltages making this type of operational amplifier circuit a Subtractor.

The basic differential amplifier is shown in figure



Since there are two inputs Superposition theorem can be used to find the outputvoltage.

When, $\mathbf{V_b = 0}$,

then the circuit becomes inverting amplifier, hence the output is due to $\mathbf{V_a}$ only.

$$V_{oa} = -\frac{R_f}{R_1} V_a \quad \text{----- (1)}$$

Similarly

When, $\mathbf{V_a = 0}$,

the configuration is a Non-inverting amplifier having a voltage divided networkat the non-inverting input.

$$V_{ob} = \left(1 + \frac{R_f}{R_1}\right) V_1 \quad \text{----- (2)}$$

but in equation (2)

$$V_1 = \left(\frac{R_2}{R_2 + R_3}\right) V_a \quad \text{----- (3)}$$

Substituting the value of V_1, in equation (2)

$$V_{ob} = \left(1 + \frac{R_f}{R_1}\right) \left(\frac{R_f}{R_2 + R_3}\right) V_a \quad \text{----- (4)}$$

In equation (4) if $R_2 = R_1$ and $R_3 = R_f$ then equation (4) can be written as

$$V_{ob} = \left(\frac{R_f}{R_1}\right) V_a \quad \text{----- (6)}$$

As per Superposition theorem sum of equation (1) and (6) is total output voltage.

$$\mathbf{V_o = \left(-\frac{R_f}{R_1}\right)(V_a - V_b)} \quad \text{----- (7)}$$

Now, differential Gain can be written as

$$\mathbf{A_D = \frac{V_o}{V_{ab}} = \frac{V_o}{V_a - V_b} = -\frac{R_f}{R_1}} \quad \text{----- (8)}$$

UNIT-I

CHARACTERISTICS OF OP-AMP

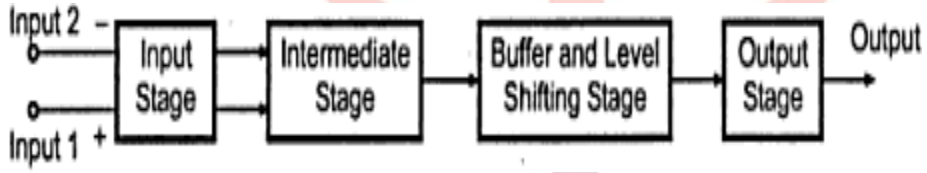
2.1 Ideal OP-AMP

An ideal OP-AMP would have the following characteristics:

1. The input resistance R_{IN} would be infinite
2. The output resistance R_{OUT} would be zero
3. The voltage gain, V_G would be infinite
4. The bandwidth (how quickly the output will follow the input) would be infinite
5. If the voltages on the two inputs are equal than the output voltage is zero (If the output is not zero it is said to have an offset)

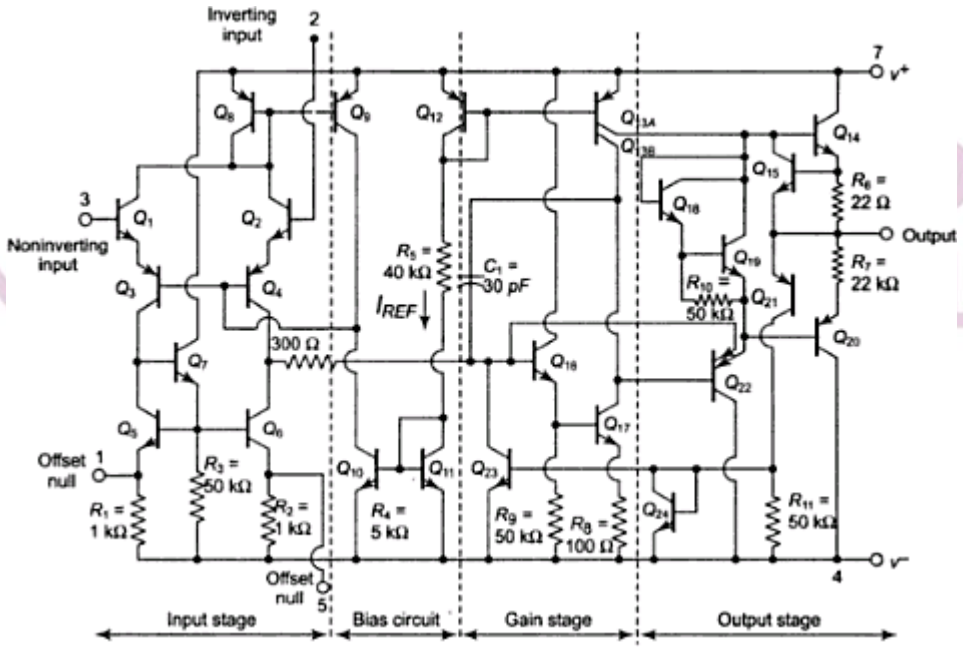
2.2. Block diagram of op-amp:

The block diagram of IC op-amp is as shown in figure



Op-amp 741:

The IC 741 is high performance monolithic op-amp IC .It is available in 8 pin, 10 pin or 14 pin configuration. It can operate over a temperature of -55 to 125 centigrade.op-amp 741 equivalent circuit is as shown in figure.



Features of IC-741

i. No frequency compensation required.
ii. Short circuit protection provided.
iii. Offset voltage null capability.
iv. Large common mode and Differential voltage range.
v. No latch up.

PSRR:

PSRR is Power Supply Rejection Ratio. It is defined as the change in the input offset voltage due to the change in one of the two supply voltages when other voltage is maintained constant. It's ideal value should be Zero.

Slew Rate:

The maximum rate of change of output voltage with respect to time is called Slew rate of the Op-amp.

It is expressed as, $S = \text{—}_{max}$ and measured in V/sec.

The Slew rate equation is, $S = 2\pi f V_m$ V/sec

Frequency compensation technique:

In application where one desires large bandwidth and lower closed loop gain, suitable compensation technique are used: Two types of compensation techniques are used

1. External compensation
2. Internal compensation

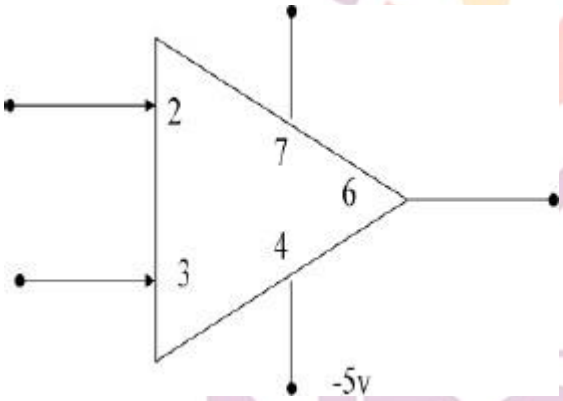
UNIT II

APPLICATIONS OF OP-AMPS

OPERATION AMPLIFIER

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage. It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

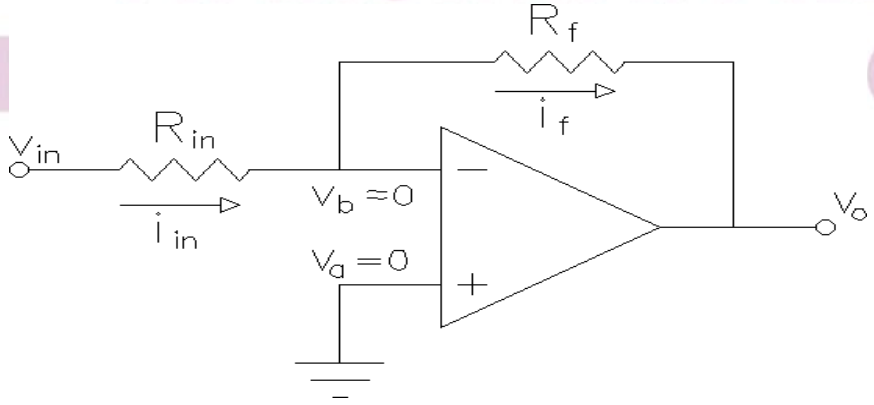
Op-amp symbol



Ideal characteristics of OPAMP

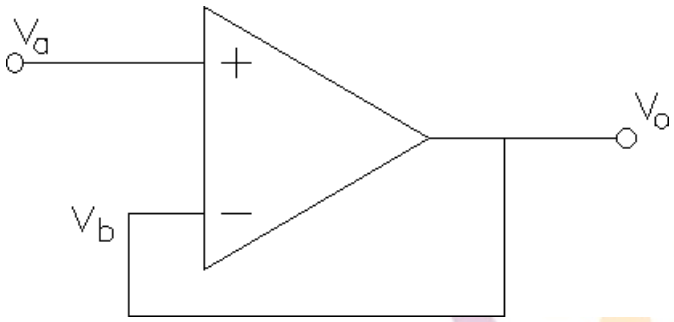
1. Open loop gain infinite
2. Input impedance infinite
3. Output impedance low
4. Bandwidth infinite
5. Zero offset, ie, Vo=0 when V1=V2=0

Inverting Op-Amp



$$V_{OUT} = -V_{IN}\frac{R_f}{R_1}$$

Voltage follower



$$V_{OUT} = V_{IN}$$

DC characteristics

Input offset current

The difference between the bias currents at the input terminals of the op- amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents

Input offset voltage

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage

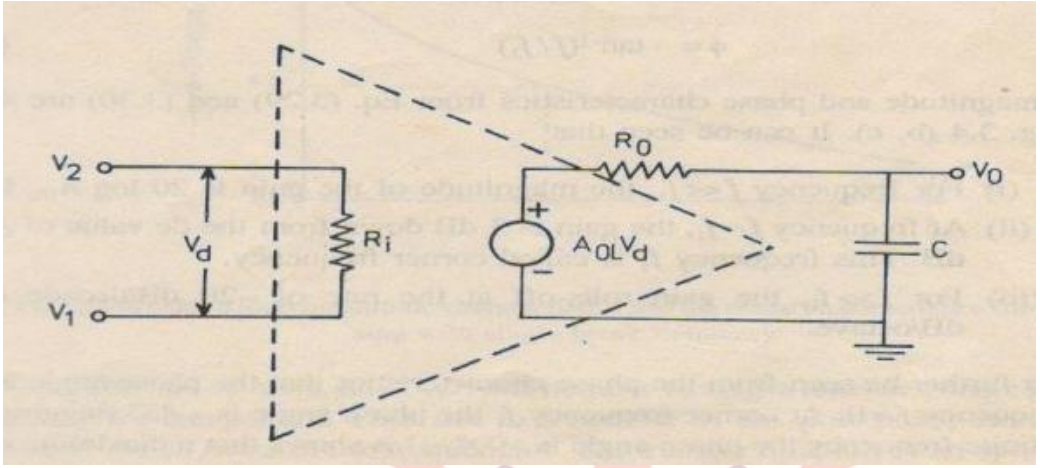
Input bias current

Input bias current IB as the average value of the base currents entering into terminal of an op-amp

$$\mathbf{I_B = I_B^+ + I_B^-}$$

AC characteristics

Frequency Response



HIGH FREQUENCY MODEL OF OPAMP

Need for frequency compensation in practical op-amps

• Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.

• Compensating networks are used to control the phase shift and hence to improve the stability

Frequency compensation methods

• Dominant- pole compensation

• Pole- zero compensation

Slew Rate

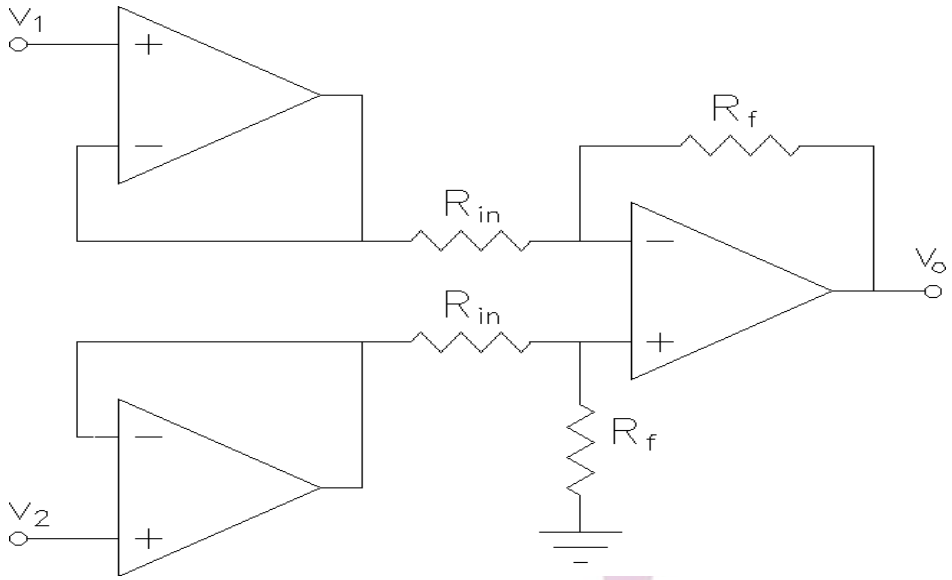
• The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage.

• An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage

Instrumentation Amplifier

In a number of industrial and consumer applications, the measurement of physical quantities

is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

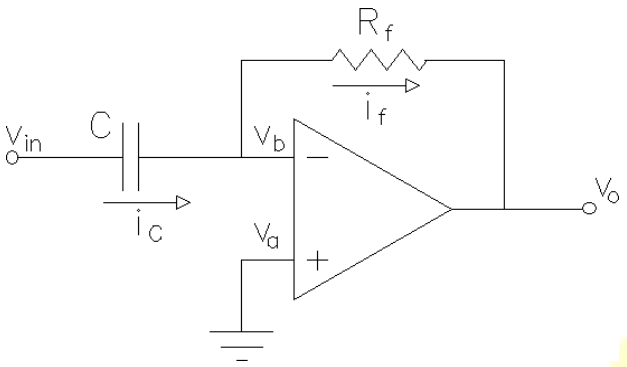


Features of instrumentation amplifier

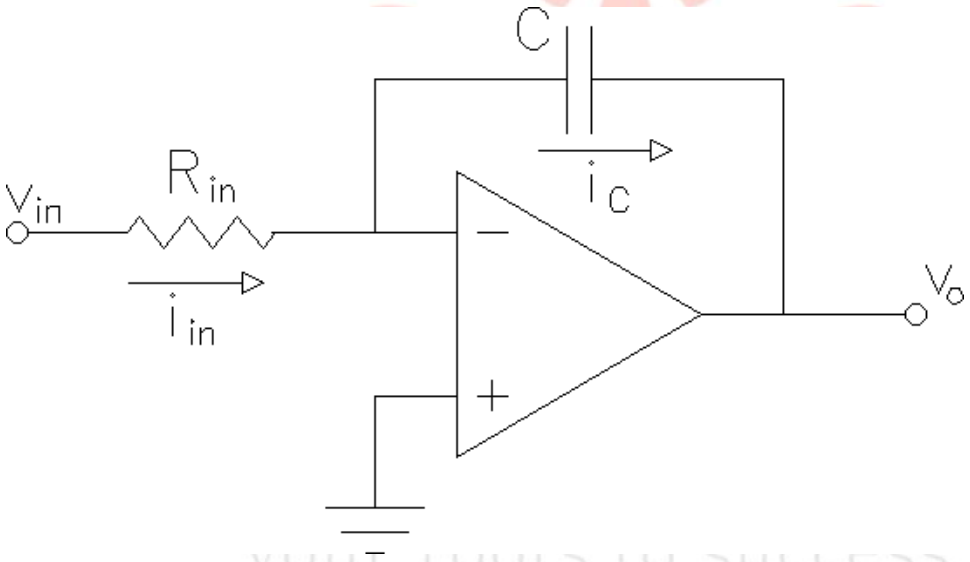
1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co- efficient
4. low dc offset
5. low output impedance

Differentiator

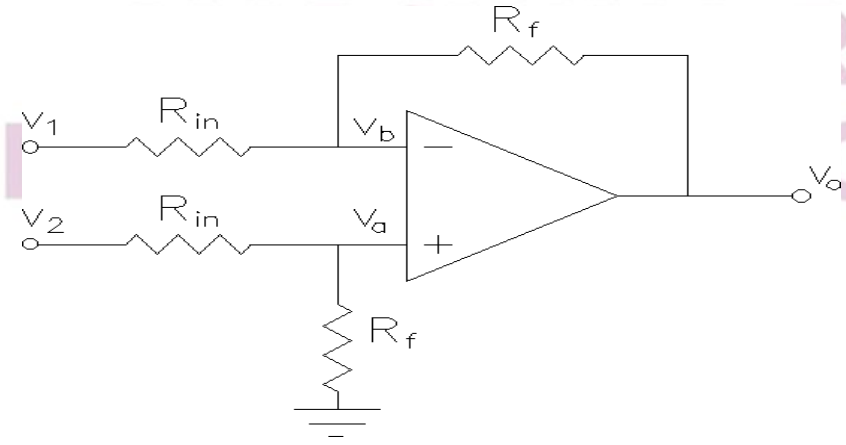
The circuit which produces the differentiation of the input voltage at its output is called differentiator. The differentiator circuit which does not use any active device is called passive differentiator. While the differentiator using an active device like op-amp is called an active differentiator.



Integrator:



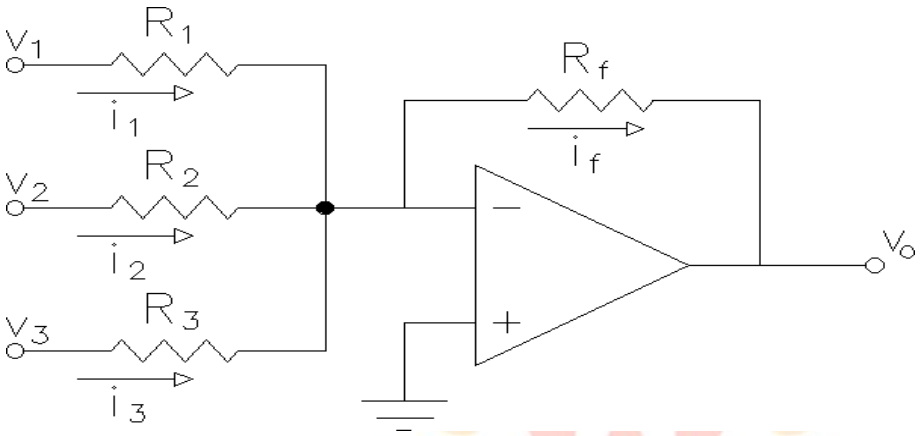
Differential amplifier:



This circuit amplifies only the difference between the two inputs. In this circuit there are two

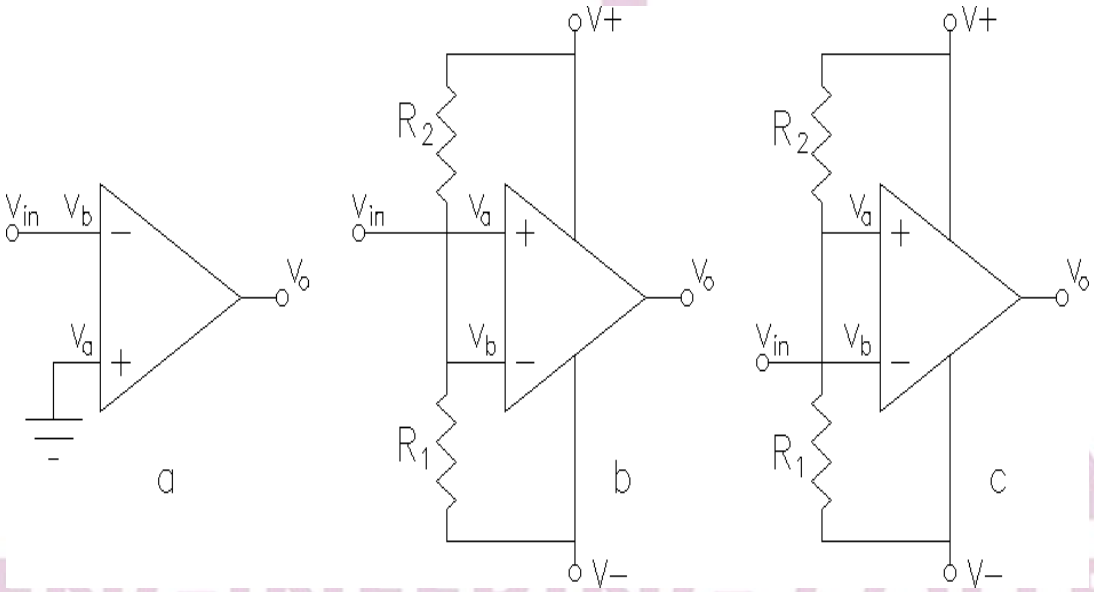
resistors labeled R IN Which means that their values are equal. The differential amplifier amplifies the difference of two inputs while the differentiator amplifies the slope of an input

Summer:



Comparator:

A comparator is a circuit which compares a signal voltage applied at one input of an op- amp with a known reference voltage at the other input. It is an open loop op - amp with output.



Applications of comparator:

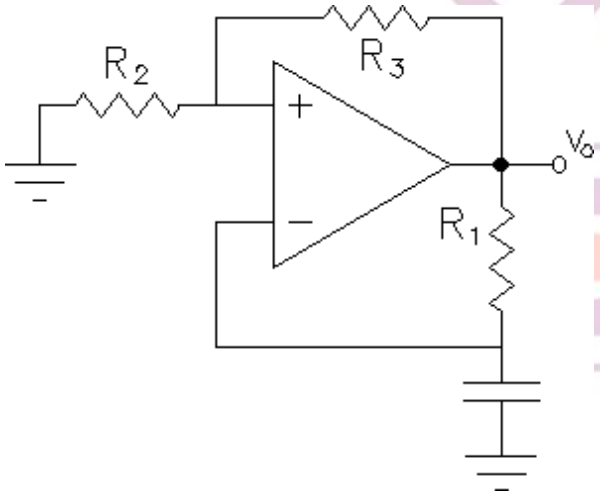
1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector

3.15 Triangular wave Generator:

The output of the integrator is triangular if the input is a square wave. This means that a triangular wave generator can be formed by simply connecting an integrator to the square wave generator.

3.17 Square wave generator:

Square wave outputs are generated when the op-amp is forced to operate in the saturated region. That is, the output of the op-amp is forced to swing repetitively between positive saturation and negative saturation. The square wave generator is also called as free-running or Astable mutivibrator



Explain Instrumentation Amplifier in detail. OR

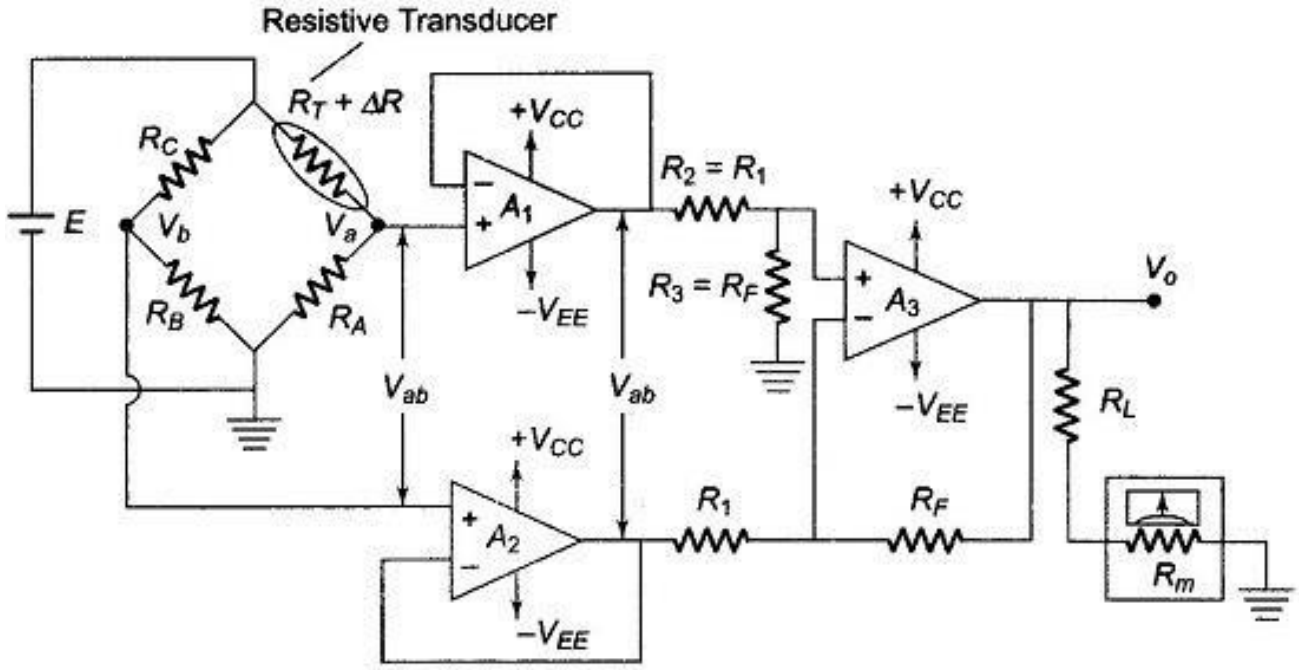
Draw and explain the circuit diagram of Instrumentation Amplifier using transducer bridge which is consisting of Thermistor in one of it's arm of bridge. OR

Explain differential Instrumentation Amplifier with transducer bridge

Simplified circuit of a Differential Instrumentation Amplifier with Transducer Bridge is as shown in figure.

In this circuit a resistive transducer/Thermistor (whose resistance changes as a function of some physical energy/Temperature) is connected to one arm of the bridge.

Let R_T be the resistance of the transducer and ΔR the change in resistance of the resistive transducer. Hence the total resistance of the transducer is $(R_T \pm \Delta R)$.



The condition for bridge balance is $\mathbf{V_b = V_a}$, i.e. the bridge is balanced when $V_b = V_a$, or when,

$$\frac{R_B(E)}{R_B + R_C} = \frac{R_A(E)}{R_A + R_T}$$

$$\text{Therefore,} \quad \frac{R_c}{R_B} = \frac{R_T}{R_A}$$

The bridge is balanced at a desired ***reference condition***, which depends on the specific value of the physical quantity to be measured. Under this condition, resistors R_A, R_B and R_C are so selected that they are equal in value to the transducer resistance R_T. (The value of the physical quantity normally depends on the transducers characteristics, the type of physical quantity to be measured, and the desired applications.)

Initially the bridge is balanced at a desired reference condition. As the physical quantity to be measured changes, the resistance of the transducer also changes, causing the bridge to be unbalanced ($V_b \neq V_a$). Hence, the output voltage of the bridge is a function of the change in the resistance of the transducer. The expression for the output voltage V_0, in terms of the change in resistance of the transducer is calculated as follows.

Let the change in the resistance of the transducer be ΔR. Since R_B and R_C are fixed resistors, the voltage V_b is constant, however, the voltage V_a changes as a function of the change in the transducers resistance.

Therefore, applying the voltage divider rule we have

$$V_a = \frac{R_A(E)}{R_A + (R_T + \Delta R)} \text{ and } V_b = \frac{R_B(E)}{R_B + R_C}$$

The output voltage across the bridge terminal is V_{ab}, given by $V_{ab}=V_a-V_b$

Therefore,

$$V_{ab} = \frac{R_A(E)}{R_A + (R_T + \Delta R)} - \frac{R_B(E)}{R_B + R_C}$$

$$R_A = R_B = R_C = R_T = R, \text{ then}$$

$$V_{ab} = \frac{R(E)}{2R + \Delta R} - \frac{R(E)}{2R} = E\left(\frac{R}{2R + \Delta R} - \frac{1}{2}\right)$$

$$V_{ab} = E\left(\frac{2R - 2R - \Delta R}{2(2R + \Delta R)}\right) = \frac{-\Delta R(E)}{2(2R + \Delta R)}$$

The output voltage V_{ab} of the bridge is applied to the Differential Instrumentation Amplifier through the voltage followers to eliminate the loading effect of the bridge circuit. The gain of the basic amplifier is (R_F/R_1) and therefore the output voltage V_o of the circuit is given by

$$V_o = V_{ab}\left(\frac{R_F}{R_1}\right) = \frac{-\Delta R(E)}{2(2R + \Delta R)} \times \frac{R_F}{R_1}$$

It can be seen from the above equation that V_o is a function of the change in resistance ΔR of the transducer. Since the change is caused by the change in a physical quantity, a meter connected at the output can be calibrated in terms of the units of the physical quantity.

Applications of Instrumentation Amplifier with Transducer Bridge

We shall now consider some important applications of instrumentation amplifiers using resistance types transducers. In these transducers, the resistance of the transducer changes as a function of some physical quantity. Commonly used resistance transducers are thermisistors, photoconductor cells, and strain gauges.

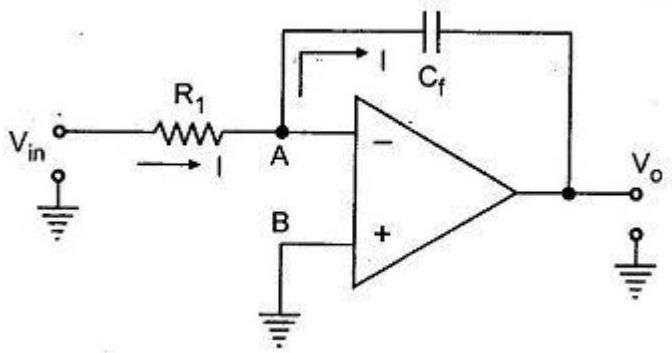
(i) Temperature Indicators Using Thermistor
(ii) Light Intensity Meter
(iii) Analog Weight Scale

Explain Integrator circuit in detail. OR

Draw circuit diagram of Integrator using Op. Amp. and derive the equation of output voltage. Also draw the output waveform if input is (i) Sine wave and (ii) Square wave. OR

Draw circuit diagram of Integrator using Op. Amp and explain it with necessary frequency response and derivations. Also draw practical Integrator circuit.

An integrator is the circuit in which the output voltage waveform is the integral of the input voltage waveform. It can be obtained by replacing feedback resistor by ***feedback capacitor*** in basic inverting amplifier. Input signal, which can be applied at the inverting terminal i.e. pin – 2 of the op-amp through resistor Rin. A feedback capacitor Cfis connected between the output terminal i.e. pin – 6 and the inverting terminal i.e. pin –2 of the op-amp.



The non-inverting terminal i.e. pin – 3 of the op-amp is grounded either directly or through a resistor which is a parallel combination of input resistor Rin and feedback resistor Rf. Figure 1 shows Basic Integrator Circuit.

The output of the op-amp will then be integrated version of the input.

DESIGN EQUATION *:* -

Applying KCL at inverting node,

$$\mathbf{I_{in} = I_B + I_F}$$

As input impedance of op-amp is very large, bias current I_B =0. Therefore,

$$\mathbf{I_{in} = I_F = I}$$

The current through resistor R_1 can be given as

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1}$$

---- (1)

The current through capacitor can be given as

$$I = C_f \frac{d(V_A - V_o)}{dt}$$

$$I = -C_f \frac{dV_o}{dt}$$

-----(2)

Because of virtual ground concept V_A=V_B=0 in equation (1) and (2).

Now comparing equation (1) and (2)

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt} \qquad \text{----(3)}$$

Integrating both sides of equation (3)

$$\int_0^t \frac{V_{in}}{R_1} dt = -C_f \int \frac{dV_o}{dt} . dt$$

$$\text{i.e.} \quad \int_0^t \frac{V_{in}}{R_1} dt = -C_f V_o \qquad \text{---- (4)}$$

$$\therefore \quad V_o = -\frac{1}{R_1 C_f} \int_0^t V_{in}\, dt + V_o(0)$$

$$\boxed{V_o = -\frac{1}{R_1 C_f} \int_0^t V_{in}\, dt} \qquad \text{---- (5)}$$

Equation (5) indicates that output is integration of input voltage. Hence this circuit willwork as an integrator circuit.

Where $V_o(0)$ is constant of integration and it indicates initial value of output voltage attime t=0.

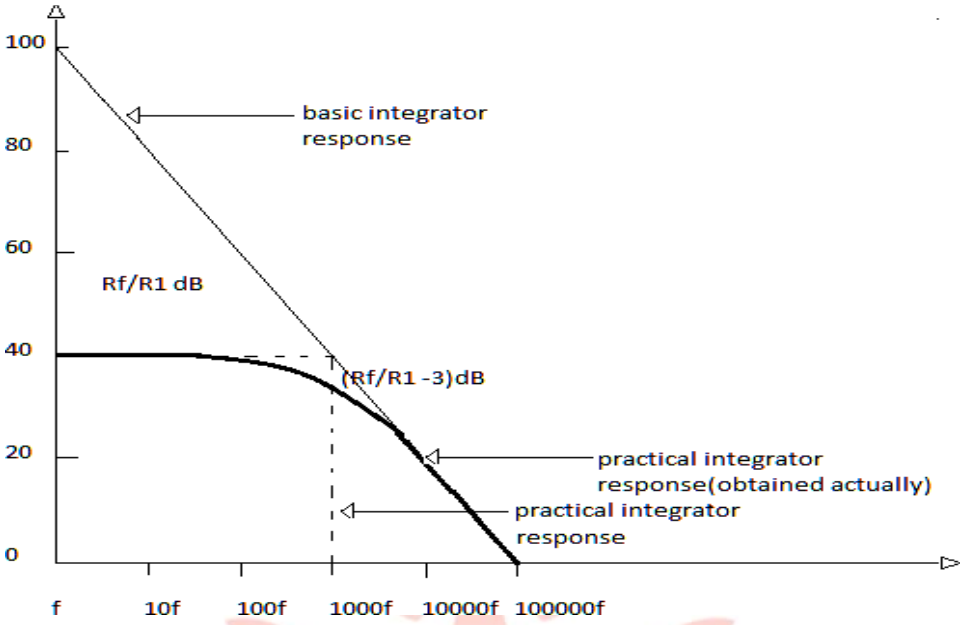
Frequency Response of Integrator:

Frequency response is graph relating Gain and Frequency.

Capacitive reactance **Xc** = $\frac{\mathbf{1}}{\mathbf{2\pi f C}}$

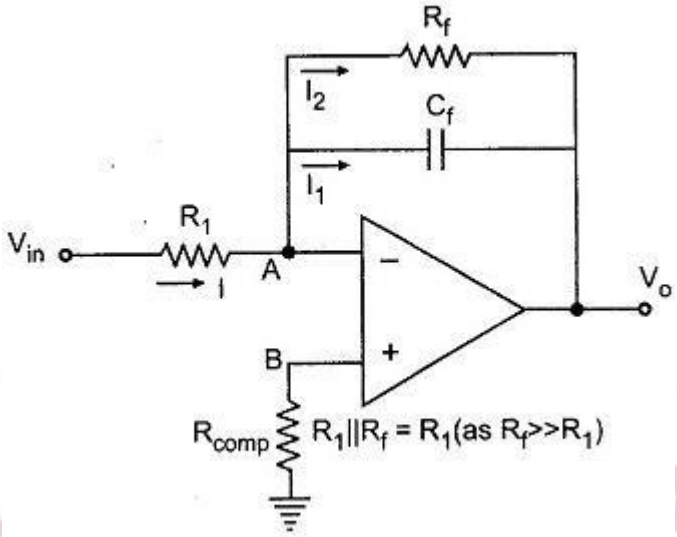
As frequency is increases, Xc and gain will decreases.

But at low frequency capacitive reactance Xc is high, so gain is very large and circuit becomes unstable at low frequency input signal. To control the gain at low frequency, a Resistor Rf is required to be connected in parallel with Cf in practical integrator circuit. Frequency response of Ideal/Basic integrator and practical integrator circuit is as shown in figure.



Frequency Response of Basic & Practical Integrator

***PRACTICAL INTEGRATOR CIRCUIT*:**



Practical Integrator circuit

DESIGN:

Frequency at which gain starts decreases is called gain limiting frequency and is givenby equation

$$f_a = \frac{1}{2\Pi R_f C_f}$$

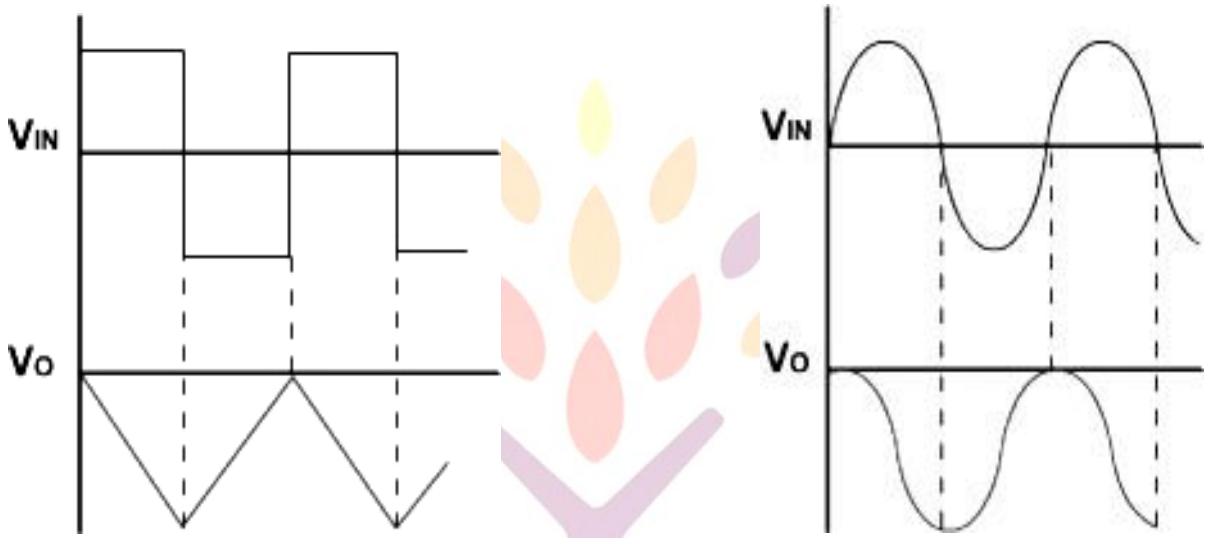
The frequency at which the gain is 0 dB (Unity) is given by equation

$$f_b = \frac{1}{2\Pi R_1 C_f}$$

Generally $\mathbf{f_b = 20\ f_a}$

Now selecting standard value of capacitor Cf we can determine the value of R1 and Rfusing equation of $\mathbf{f_a}$ and $\mathbf{f_b}$ to design Integrator of particular frequency range.

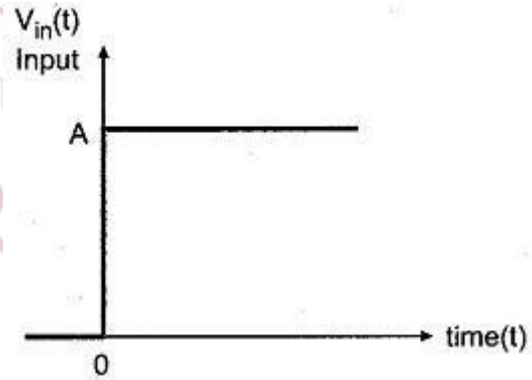
INPUT & OUTPUT WAVE FORMS : -



Draw the output wave form if unit step input is applied to an integrator as shown in figure.

Let the input waveform is of step type, with a magnitude of A units as shown in thefigure.

For simplicity of understanding, assume that the time constant $R_1C_f = 1$ and the initialvoltage $V_0(0)$ = OV.



Mathematically the step input can be expressed as,

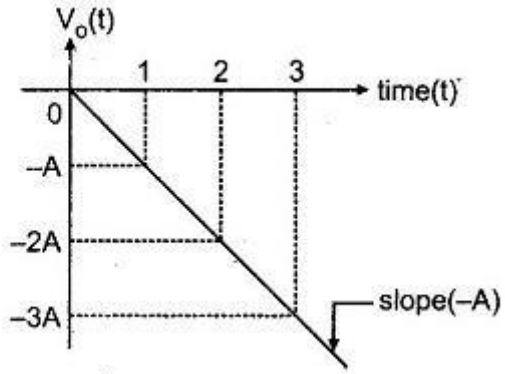
$$V_{in}(t) = A \text{ for } t \geq 0$$
$$= 0 \text{ for } t < 0$$

From above equation with $R_IC_f = 1$ and $V_0(0) = 0$,

$$V_o(t) = -\int_0^t V_{in}(t)\,dt = -\int_0^t A\,dt = -A\int_0^t dt = -A\,[t]_0^t$$

$$V_o(t) = -At$$

Now the output waveform can be drawn as follow:



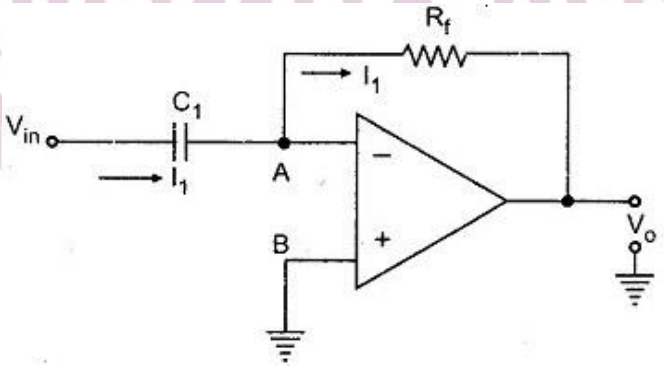
Thus output waveform is a straight line (negative going Ramp) with a slope of -A where A is magnitude of the step input. The output waveform is shown in the figure.

Explain Differentiator circuit in detail. OR

Draw circuit diagram of Differentiator using Op. Amp. and derive the equation of output voltage. Also draw the output waveform if input is (i) Sine wave, (ii) Square wave and (iii) Triangular wave. OR

Draw circuit diagram of Differentiator using Op. Amp and explain it with necessary frequency response and derivations. Also draw practical Differentiator circuit.

The circuit which produces the differentiation of the input voltage at its output is called ***Differentiator***. The differentiator using an active device like op-amp is called an active Differentiator. Let us discuss first the operation of Ideal/Basic Differentiator circuit.



The active differentiator circuit can be obtained by exchanging the positions of R and C in the basic integrator circuit. The op-amp differentiator circuit is shown in the figure.

The node B is grounded. The node A is also at the ground potential because of virtual ground, hence $V_A = 0$.

DESIGN EQUATION *:* -

Applying KCL at inverting node,

$$\mathbf{I_{in} = I_B + I_F}$$

As input impedance of op-amp is very large, bias current $I_B = 0$. Therefore,

$$\mathbf{I_{in} = I_F = I_1}$$

The current through capacitor C_1 can be given as

$$I_1 = C_1 \frac{d(V_{in} - V_A)}{dt} = C_1 \frac{d V_{in}}{dt} \quad \text{---- (1)}$$

The current through resistor R_f can be given as

$$I = \frac{(V_A - V_o)}{R_f} = -\frac{V_o}{R_f} \quad \text{-----(2)}$$

Because of virtual ground concept $V_A = V_B = 0$ in equation (1) and (2).

Now comparing equation (1) and (2)

$$C_1 \frac{d V_{in}}{dt} = -\frac{V_o}{R_f} \quad \text{----- (3)}$$

Hence, $$\boxed{V_o = -C_1 R_f \frac{d V_{in}}{dt}} \quad \text{----------(4)}$$

Equation (4) indicates that output is differentiation of input voltage. Hence this circuit will work as an differentiator circuit.

Frequency Response of Differentiator:

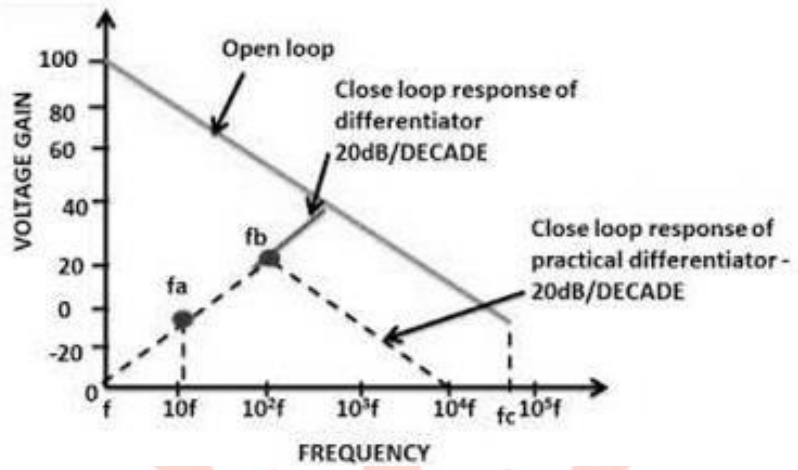
Frequency response is graph relating Gain and Frequency.

Capacitive reactance $\mathbf{Xc} = \frac{\mathbf{1}}{\mathbf{2\pi f C}}$

As frequency is increases, Xc will decreases and gain will increase.

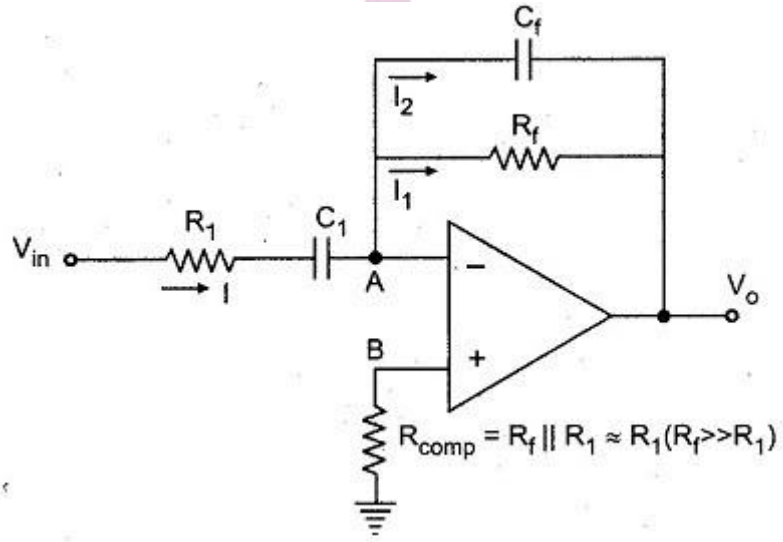
At low frequency capacitive reactance Xc is high, so gain is low and circuit is stable. But as the frequency is increasing, Xc will decrease which cause the gain to increase. Thus at high frequency input signal, circuit becomes unstable.

So, gain is required to be controlled at high frequency. To control the gain at high frequency, a Resistor R_1 is required to be connected in series with input capacitor C_1 in practical Differentiator circuit. Also a feedback resister R_f is to be connected in parallel with C_f. Frequency response of Ideal/Basic differentiator and practical differentiator circuit is as shown in figure.



Frequency Response of Basic & Practical Differentiator

***PRACTICAL DIFFERENTIATOR CIRCUIT*:**



Practical Differentiator circuit

DESIGN*:*

The frequency at which the gain is 0 dB (Unity) is given by equation

$$f_a = \frac{1}{2\Pi R_f C_1}$$

Frequency at which gain starts decreases is called gain limiting frequency and is givenby equation

$$f_b = \frac{1}{2\Pi R_1 C_1}$$

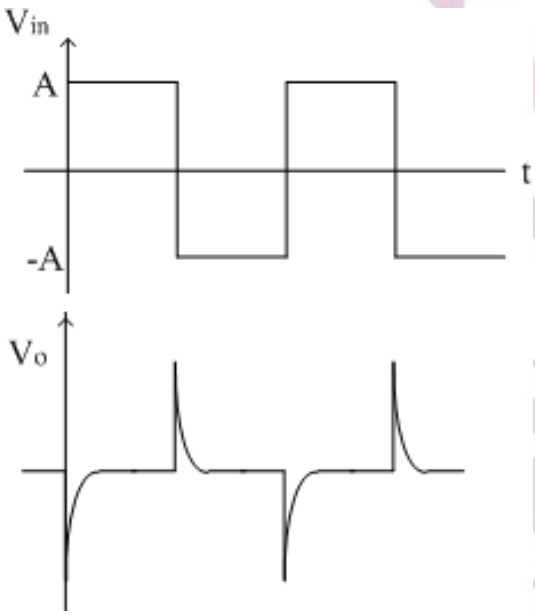
Also gain is controlled by C_f and R_f. Hence gain limiting frequency can be given by equation.

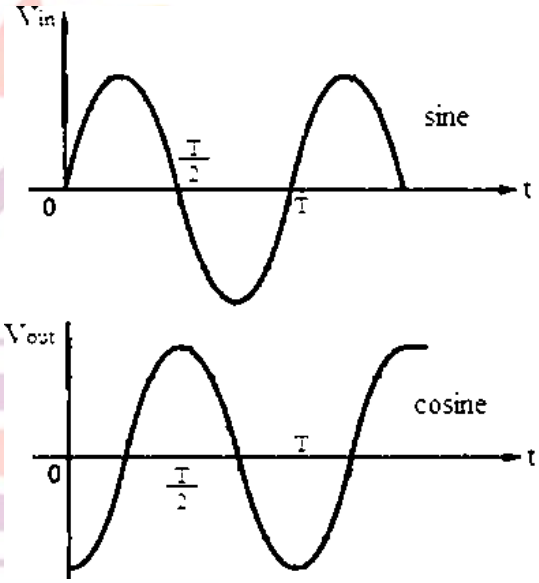
Generally $\mathbf{f_b = 20\ f_a}$

$$f_b = \frac{1}{2\Pi R_f C_f}$$

Now selecting standard value of capacitor C_1 we can determine the value of C_f , R_1 and R_f using equation of $\mathbf{f_a}$ and $\mathbf{f_b}$ to design differentiator of particular frequency range.

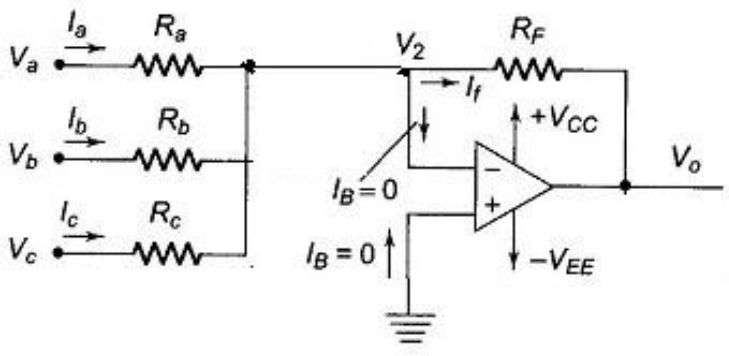
INPUT & OUTPUT WAVE FORMS : -





Explain Summing, Scaling and Averaging amplifier using Op. Amp.

Figure shows an Summing Amplifier Circuit in inverting configuration with three inputs V_a, V_b, V_c. Depending on the relation between R_a, R_b, R_c and R_F, the circuit can be used as a Summing amplifier, Scaling amplifier or Average amplifier.



Using Kirchoff's circuit equation, we have $l_a + l_b + l_c = I_B + I_f$. But $I_B \equiv 0$ and $V_1 \equiv V_2 \equiv 0$(Virtual ground)

Therefore,

$$\mathbf{I_a + I_b + I_c = I_f} \text{----------} (1)$$

$$\frac{V_a - V_2}{R_a} + \frac{V_b - V_2}{R_b} + \frac{V_c - V_2}{R_c} = \frac{V_2 - V_o}{R_f} \quad \text{---- (2)}$$

As V_2 is virtual ground, $V_2 = 0$. Hence equation (2) is

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = \frac{-V_o}{R_f} \quad \text{---- (3)}$$

So,

$$\boxed{\mathbf{V_o = -\left[\frac{R_f V_a}{R_a} + \frac{R_f V_b}{R_b} + \frac{R_f V_c}{R_c}\right]}} \quad \text{---- (4)}$$

(i) Summing Amplifier:

In equation (4) if $\boldsymbol{R_a = R_b = R_c = R_f = R}$ then equation (4) is

$$\boxed{V_o = -[V_a + V_b + V_c]} \quad \text{---- (5)}$$

Thus circuit will behaves as Summing Amplifier which gives output that is sum of allthe inputs. It is also called ***Adder circuit***

(ii) Scaling Amplifier:

In equation (4) if $\boldsymbol{R_a \neq R_b \neq R_c \neq R_f}$ then equation (4) is

$$\boxed{V_o = -\left[\frac{R_f V_a}{R_a} + \frac{R_f V_b}{R_b} + \frac{R_f V_c}{R_c}\right]} \quad \text{---- (6)}$$

Thus circuit will behaves as Scaling Amplifier in which every input is amplified by different scale/weight. Gain of every input is different.

(iii) Averaging Amplifier:

In equation (4) if $\boldsymbol{R_a = R_b = R_c = R}$ and $\boldsymbol{R = 3R_f}$ then equation (4) is

$$\boxed{V_o = -\frac{R_f}{R}[V_a + V_b + V_c]} \quad \text{---- (7)}$$

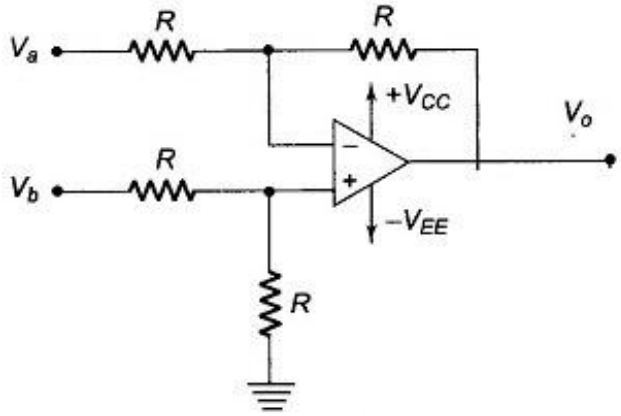
and

$$\boxed{V_o = -\left[\frac{V_a + V_b + V_c}{3}\right]} \quad \text{---- (8)}$$

Thus circuit will behaves as Average Amplifier in which output is the average ofthree inputs..

Explain Subtractor circuit using Op. Amp.

A subtractor circuit using a basic differential amplifier is as shown in figure.



By selecting the appropriate values for the external resistance, the input signal can bescaled to the desired value.

As shown in figure, all values of the external resistance are equal, and the gain of theamplifier is unity.

Therefore, the output voltage of differential amplifier with unity gain.As we know

that output voltage in differential amplifier is

$$\mathbf{V_o} = -\frac{R_f}{R_1}\,[\,V_a - V_b\,]$$

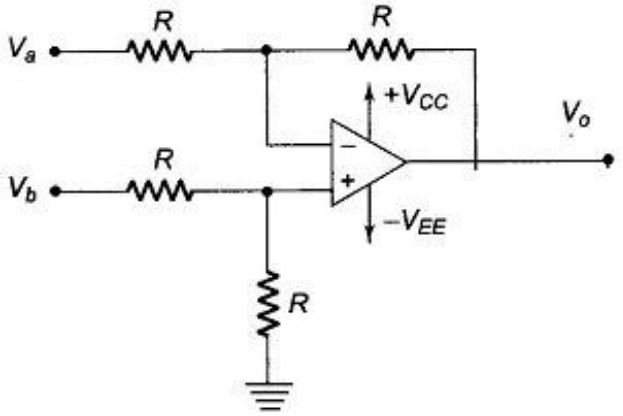
But in above circuit $\boldsymbol{R_f = R_1 = R_2 = R_3 = R}$

Hence,

$$V_o = -\,[\,V_a - V_b\,] \qquad \text{--- (1}$$

Explain Subtractor circuit using Op. Amp.

A subtractor circuit using a basic differential amplifier is as shown in figure.



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that output voltage in differential amplifier is

$$V_o = -\frac{R_f}{R_1}\,[V_a - V_b]$$

But in above circuit $R_f = R_1 = R_2 = R_3 = R$

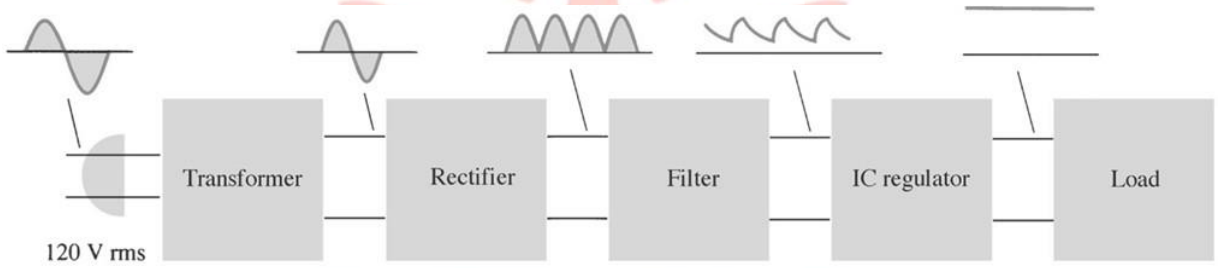
Hence,

$$V_o = -[V_a - V_b]$$

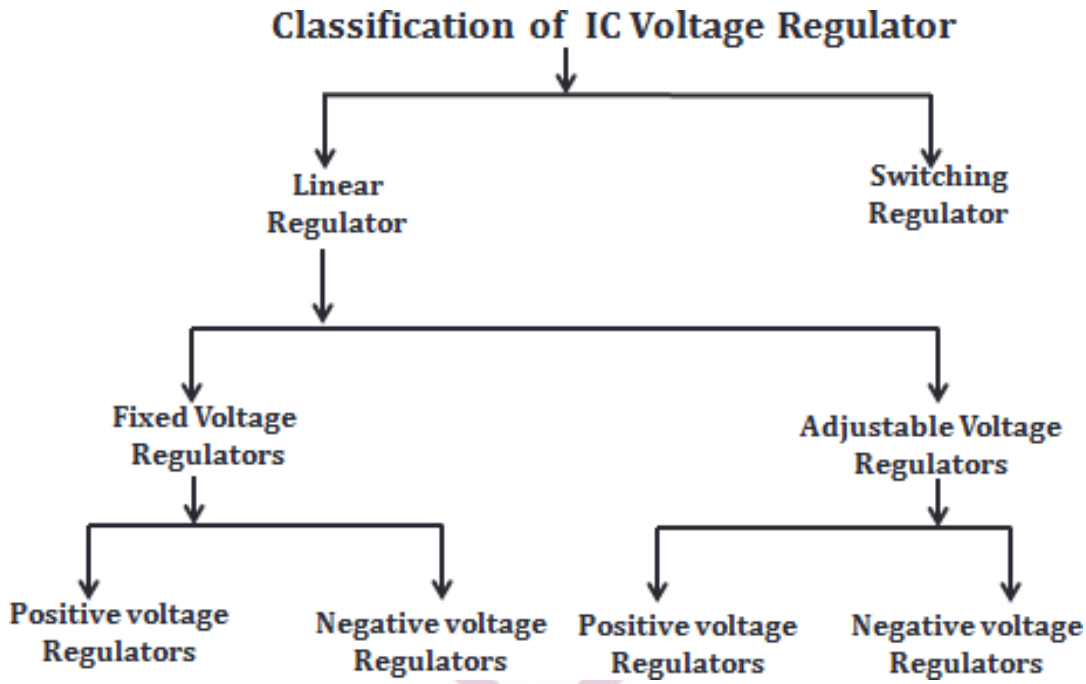
Explain IC Voltage regulators in detail. OR

Explain three terminal voltage regulators in detail.

A Voltage Regulator is a device or a circuit that is responsible for providing a steady DC Voltage to an electronic load. IC Voltage Regulator uses integrated circuits for voltage regulation.



Block diagram of a power supply which uses IC regulator is as shown in figure



Advantages of IC voltages regulators:

(1) The IC voltage regulator is conveniently used for local regulation.
(2) The IC voltage regulator is easy to use.
(3) It is most efficient and reliable.
(4) The IC voltage regulator is versatile.
(5) It is very cheap due to mass production and easily available.
(6) It is compact in size, rugged and light in weight.
(7) The power supply design becomes easy and quick.
(8) It is easily manufactured with features like built in protection, programmable output, current or voltage boosting, internal protections such as thermal shutdown, floating operation to facilitate higher output voltage etc.
(9) It has fast transient response.

IC voltage regulators/Three terminal regulator/3-T regulars:

Regulation/regulator circuits in integrated circuit form are most widely used. They are treated as a single device with associated components. These are generally three terminal devices that provide a positive or negative output.

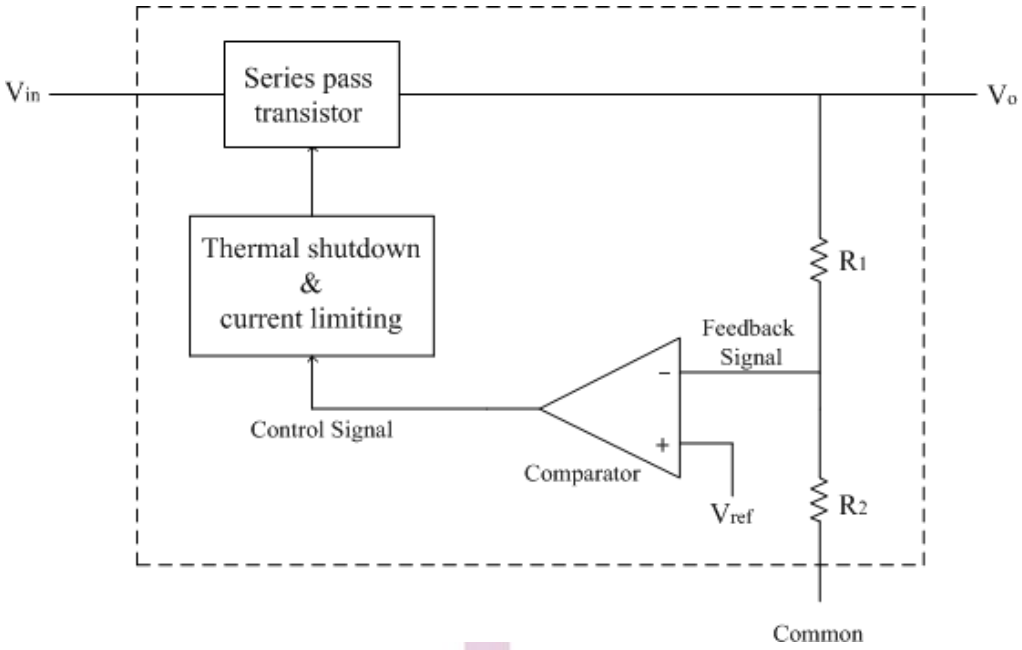
IC regulators contain the circuitry for:

- reference source
- comparator amplifier
- control device
- overload protection

The following figure shows the block diagram of three terminal IC regulator

It has three terminals.

(1) Input voltage (V_{in})
(2) Output voltage (V_o)
(3) Common terminal (Ground).



Several types of both linear (series and shunt) and switching regulators are availablein integrated circuit (IC) form.

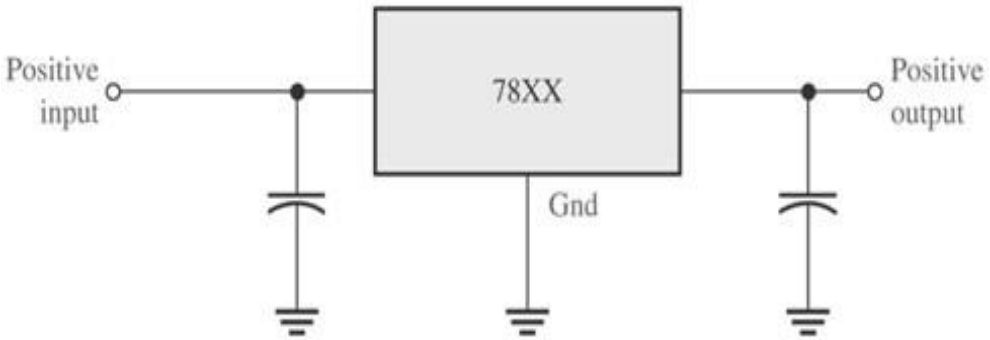
Generally, the linear regulators are three-terminal devices that provides either positive or negative output voltages that can be either fixed or adjustable

Fixed voltage regulator:

The fixed voltage regulator has an unregulated dc input voltage V_i applied to one input terminal, a regulated output dc voltage V_o from a second terminal, and the third terminal connected to ground.

Fixed-Positive Voltage Regulator

The series 78XX regulators are the three-terminal devices that provide a fixed positive output voltage.



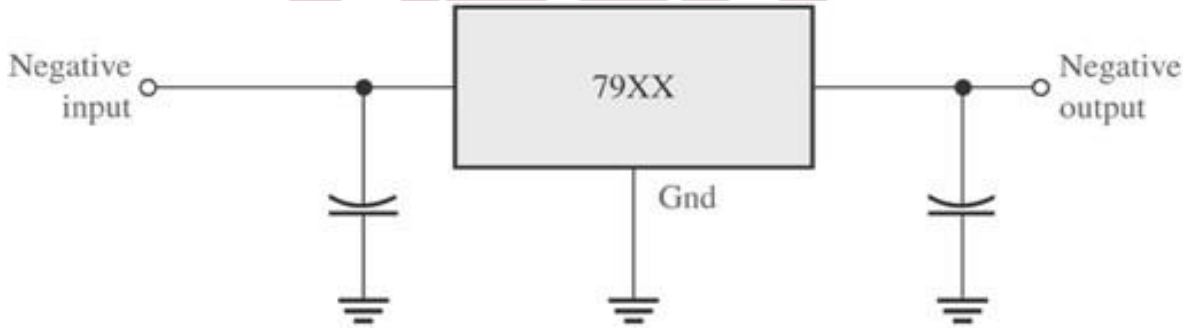
Some of the fixed positive regulator in 78XX series are given in table.

IC Part	Output Voltage (V)	Minimum V_i (V)
7805	+5	+7.3
7806	+6	+8.3
7808	+8	+10.5
7810	+10	+12.5
7812	+12	+14.5

Fixed-Negative Voltage Regulator:

The series 79XX regulators are the three-terminal IC regulators that provide a fixednegative output voltage.

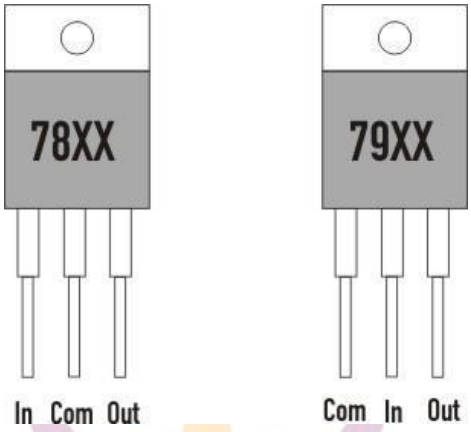
This series has the same features and characteristics as the series 78XX regulatorsexcept the pin numbers are different.



Some of the fixed negative regulator in 79XX series are given in table.

IC Part	Output Voltage (V)	Minimum V_i (V)
7905	- 5	- 7.3
7906	- 6	- 8.3
7908	- 8	- 10.5
7910	- 10	- 12.5
7912	- 12	- 14.5

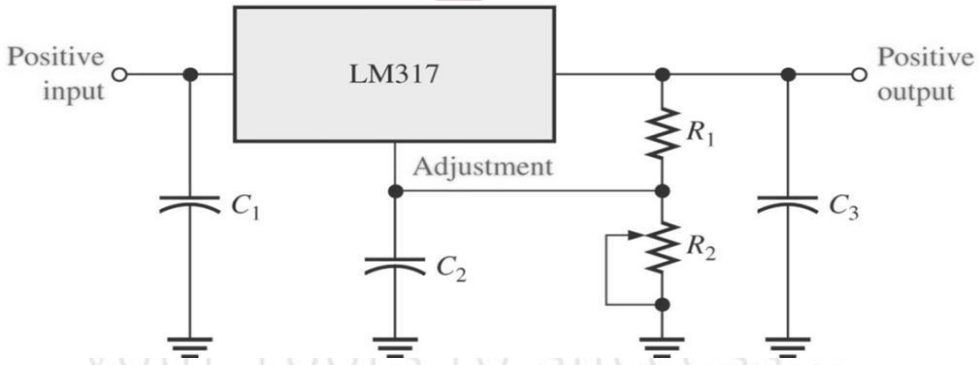
Pin configuration of 78XX and 79XX series regulator



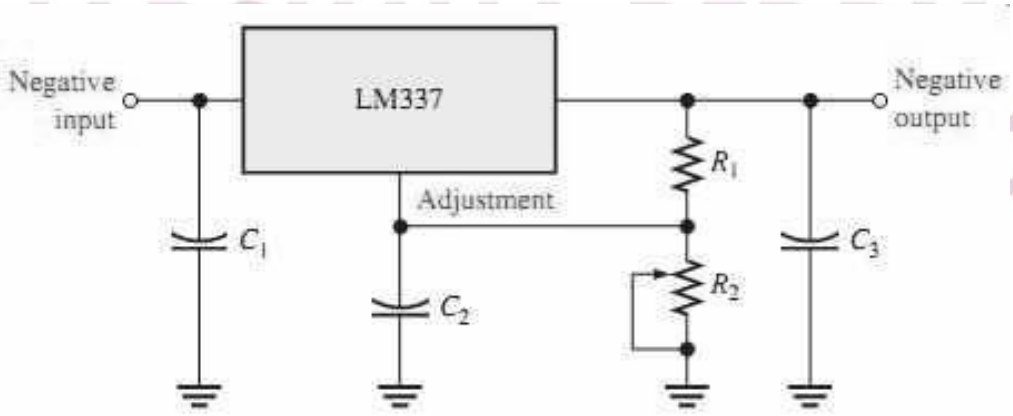
Adjustable-Voltage Regulator:

Voltage regulators are also available in circuit configurations that allow to set the output voltage to a desired regulated value.

The LM317 is an example of an positive adjustable-voltage regulator, can be operated over the range of voltage from 1.2 to 37 V.

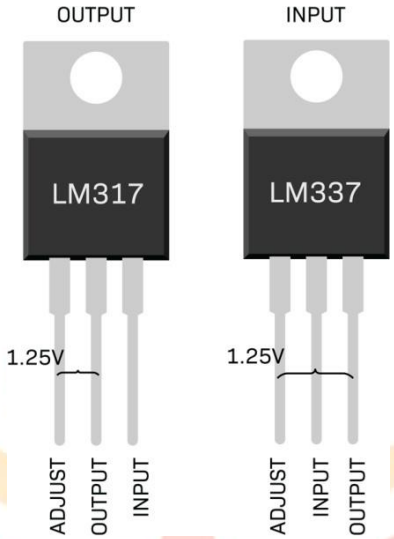


The three terminals are V_{in}, V_{out}, and Adjustment(adj).



The LM337 series of voltage regulators are a complement of LM317 series. They are negative adjustable voltage regulators. These negative voltage regulators are available in the same voltage and current options as the positive adjustable voltage regulator LM317

Pin configuration of LM317 and LM337
adjustable regulators



What is Comparator? Explain basic comparator circuit. OR

What is Comparator? Draw the circuit for Inverting and Non-inverting comparator using Op. Amp. and explain it with necessary waveform.

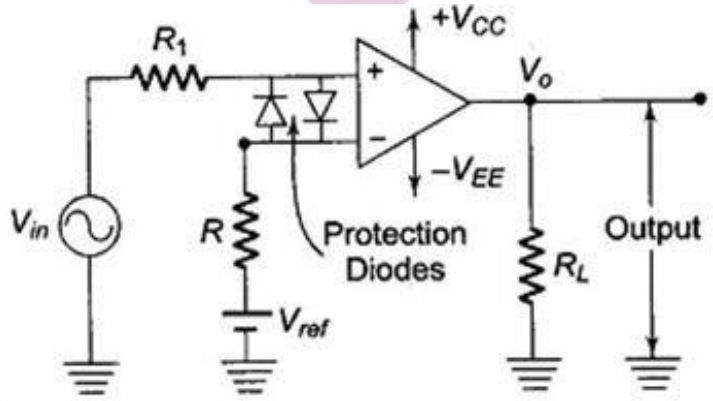
The Op Amp comparator is a circuit with two inputs and a single output. The two inputs can be compared with each other, i.e. one of them can be considered a reference terminal.

When Op. Amp. is used without feedback (open loop configuration), the amplifier output is usually in one of its saturated states.

When the non-inverting input is higher or greater than the inverting input voltage, the output of the comparator is high ($+V_{sat}$) and when the non-inverting voltage is less than the inverting voltage then output of the Comparator is low ($-V_{sat}$).

Non-inverting Comparator:

The Op. Amp. Comparator circuit shown in figure, consists of a fixed reference voltage (V_{ref}) applied to the inverting input terminal and a sinusoidal signal V_{in} applied to the non-inverting terminal.

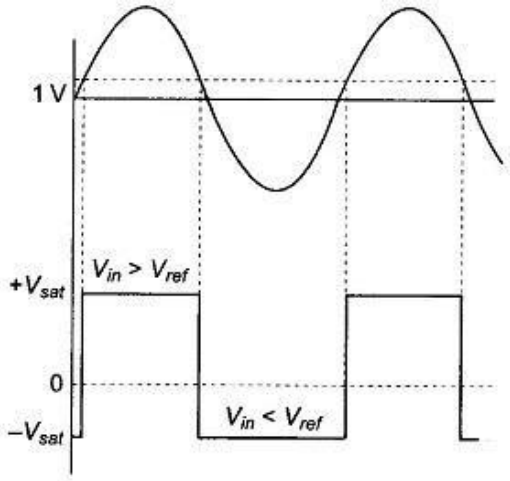


As discussed earlier, when V_{in} is greater than V_{ref} the output voltage goes to positive saturation, i.e. $V_{out} = + V_{sat} = + V_{cc}$. and when V_{in} is less than V_{ref}, the output goes to negative saturation, i.e. $V_{out} = – V_{sat} = – V_{EE}$.

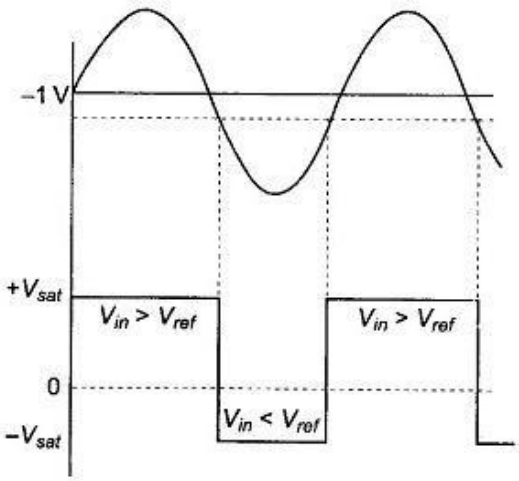
Hence the output changes from one saturation level to another. Since the sinusoidal input is applying to the non-inverting terminal, this circuit is called the non-inverting comparator.

Diodes D_1 and D_2, shown in figure are used to protect the Op. Amp. from damage due to excessive input voltage (V_{in}). The difference input voltage (V_{id}) of the Op. Amp. is clamped to either + 0.7 V or - 0.7 V because of the diodes D_1 and D_2. Hence the diodes are called clamping diodes.

Necessary input and output waveforms are also shown in figure, in case of V_{ref} is positive as well as negative.



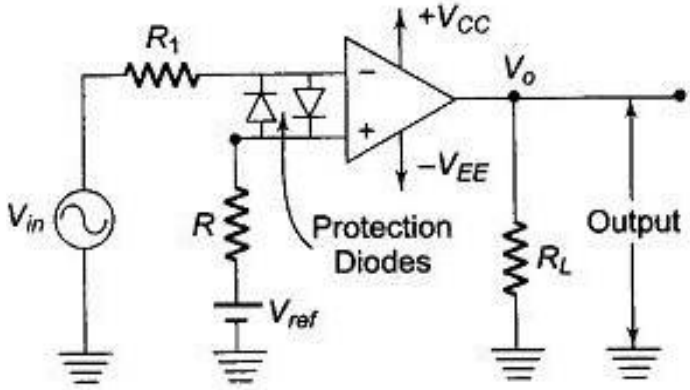
When V_{ref} is Positive



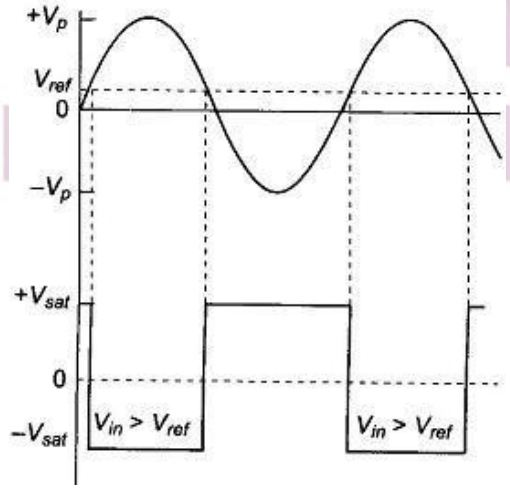
When V_{ref} is Negative

Inverting Comparator:

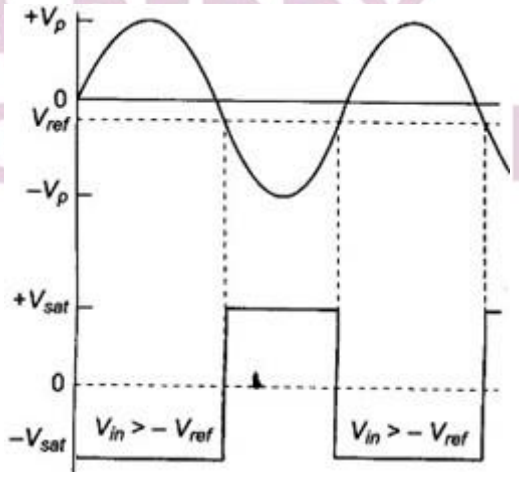
Inverting comparator can also be obtained by applying the sinusoidal input to theinverting terminal and reference voltage to non-inverting terminal.



Necessary input and output waveforms are also shown in figure, in case of V_{ref} ispositive as well as negative for inverting comparator.



When V_{ref} is Positive



When V_{ref} is Negative

Characteristics and Application of Comparator

Characteristics:

Three important characteristics of comparator are

(i) Speed of operation
(ii) Accuracy
(iii) Compatibility of output

Applications

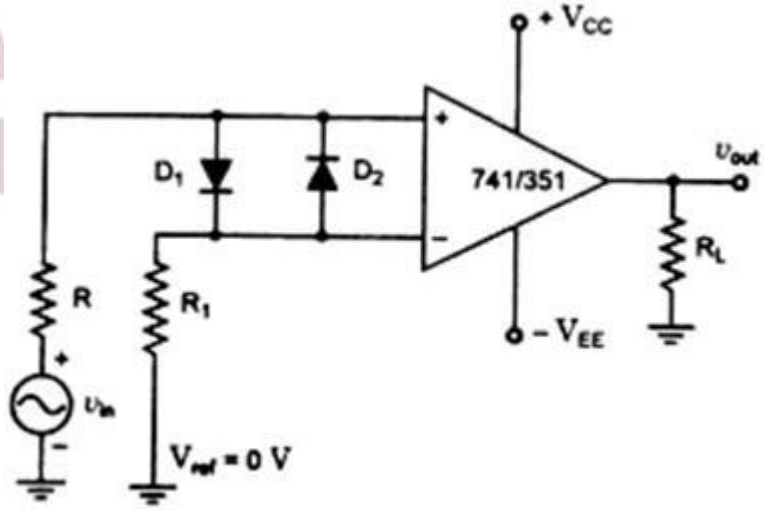
(i) Signal generation & transmission
(ii) Automatic control & measurement
(iii) A/D converter
(iv) Voltage level detector
(v) Window detector/comparator
(vi) V to F converter
(vii) Switching regulator

Explain Zero Crossing Detector.

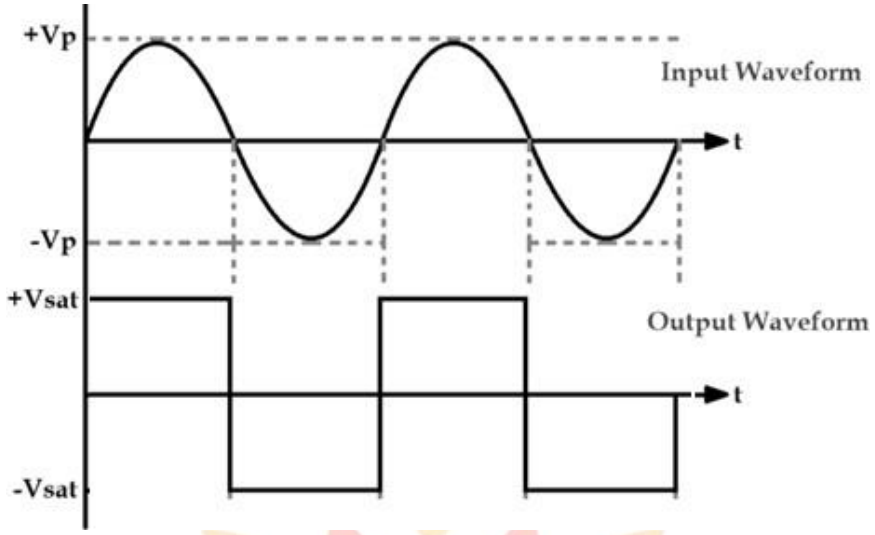
The zero crossing detector circuit in figure is seen to be simply an operational amplifier with the inverting input grounded and the signal applied to the non inverting input.

When the input is above ground level the output is saturated at its positive maximum, and when the input is below ground the output is at its negative maximum level.

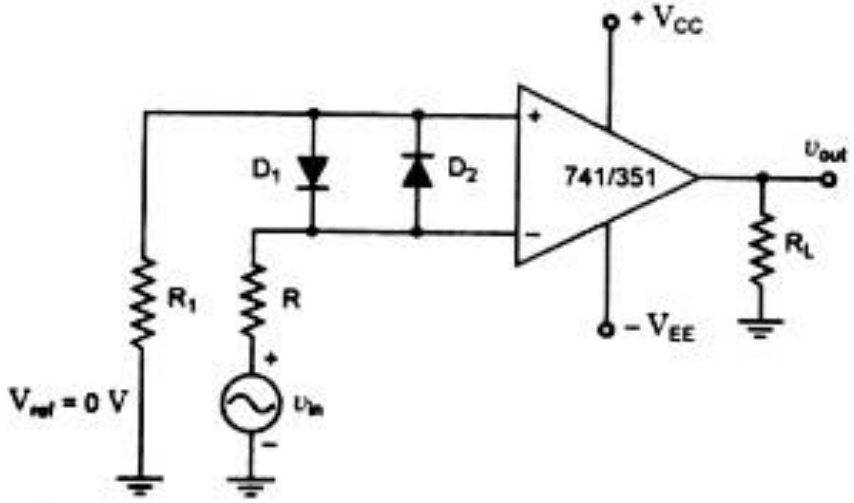
This is illustrated by the input and output waveforms which show that the output voltage changes from one extreme to the other each time the input voltage crosses zero. The input waveform could have any shape (sinusoidal, pulse, ramp, etc.), and the outputwill always be a rectangular-type wave.



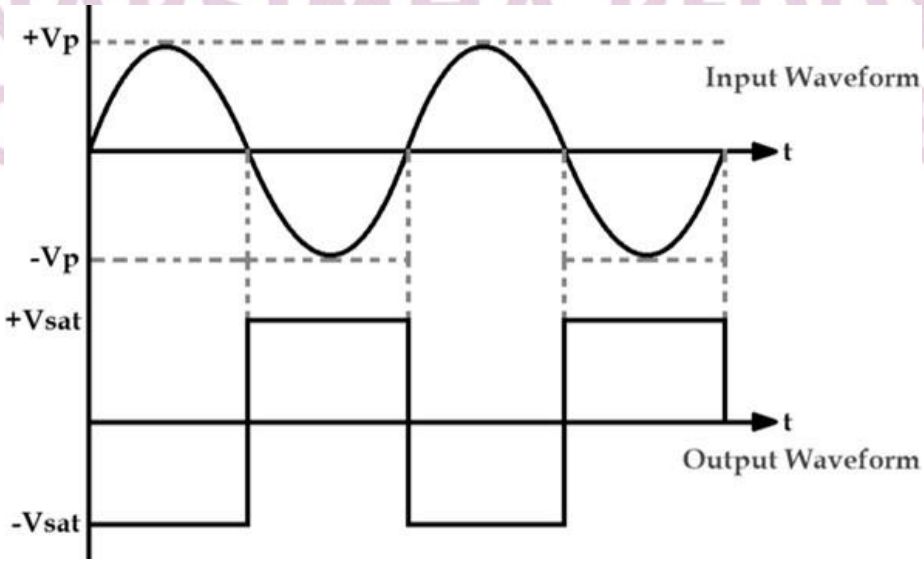
Input and output waveform for Zero crossing detector is as shown in figure



If the op-amp non-inverting input is grounded and the signal is applied to the inverting input then output is negative when the input is above ground, and vice versa. Because of the waveform inversion, this circuit is often termed an **inverter**



Input and output waveform for Zero crossing detector is as shown in figure.



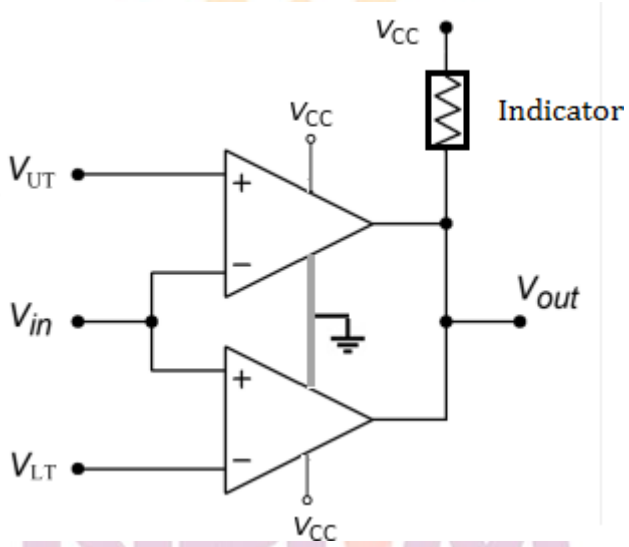
Explain Window Detector/Window comparator circuit

A **window detector circuit**, also called **window comparator circuit** or **dual edge limit detector circuits.**

It is used to determine whether an unknown input is between two precise reference threshold voltages. It employs two comparators to detect over-voltage or under- voltage.

Each single comparator detects the common input voltage against one of two reference voltages, normally upper threshold and lower threshold. Outputs detect whether the input is in the range of the so-called "window" between upper and lower threshold reference voltage.

For any value of input voltage $V_{in} > V_{LT}$ and $V_{in} < V_{UT}$, both comparator's output is high, hence

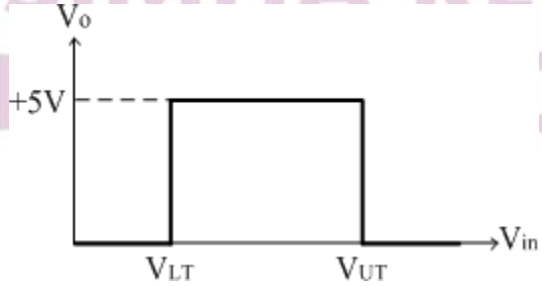


output voltage is High.

But for any value of input voltage $V_{in} < V_{LT}$ lower comparator generates output low and upper comparator generates output high, so output voltage V_{out} is low. In the same way for any value of $V_{in} > V_{UT}$, output of lower comparator is high but output of upper comparator is low, so output voltage V_{out} is low.

Hence for any value of $V_{in} < V_{LT}$ and $V_{in} > V_{UT}$, output voltage V_{out} is Low as shown in graph.

Transfer characteristic of window detector is as shown in figure.



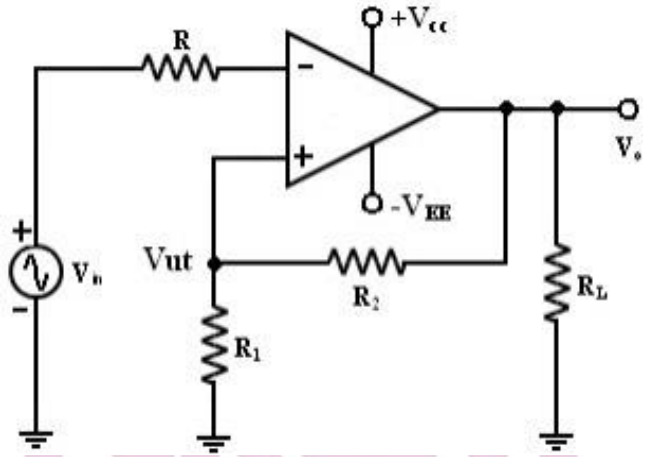
Explain Schmitt Trigger circuit. OR

Draw circuit for Inverting Schmitt Trigger. Explain it with necessary equation and also draw Hysteresis loop,

Schmitt trigger is a comparator circuit implemented by applying positive feedback to the non inverting input of a comparator or differential amplifier. It is an active circuit which converts an analog input signal to a digital output signal. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change.

In Inverting configuration, when the input is higher than a certain chosen threshold (Upper Threshold), the output is Low. When the input is lower chosen threshold (Lower Threshold), the output is High, and when the input is between the two levels, the output retains its value. This dual threshold action is called hysteresis.

A Schmitt Trigger is a circuit which converts an irregular shaped waveform to a square wave or pulse. This circuit is also called as a squaring circuit. A Schmitt trigger circuit is as shown in figure.



The input voltage V_{in} triggers (changes the state of) output V_{out} every time it exceeds certain voltage levels called upper threshold V_{ut} and lower threshold voltage V_{lt} asshown in figure.

These threshold voltages can be obtained by using the voltage divider R_1 and R_2, where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is a variable reference threshold voltage that depends on the value and the polarity of the output voltage. When $V_{out} = +V_{sat}$, the voltage across R_1 is called the upper threshold voltage,V_{ut}.

$$V_{ut} = \frac{R_1}{R_1 + R_2} \times (+V_{sat}) \qquad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

On the other hand, when $V_{out} = -V_{sat}$, the voltage across R_1 is referred to as lowerthreshold voltage, V_{lt}.

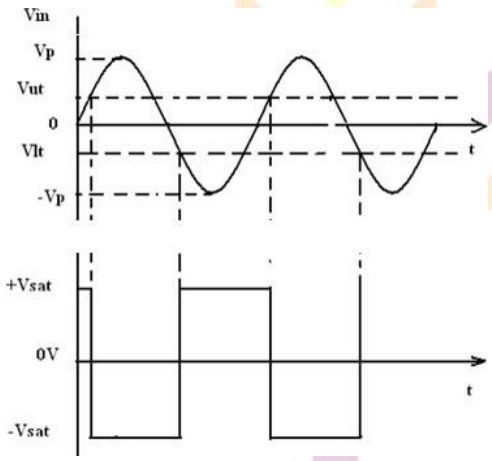
$$V_{lt} = \frac{R_1}{R_1 + R_2} \times (-V_{sat}) \qquad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The hysteresis voltage is, equal to the difference between V_{ut} and V_{lt}. Therefore,

$$V_{hy} = V_{ut} - V_{lt}$$

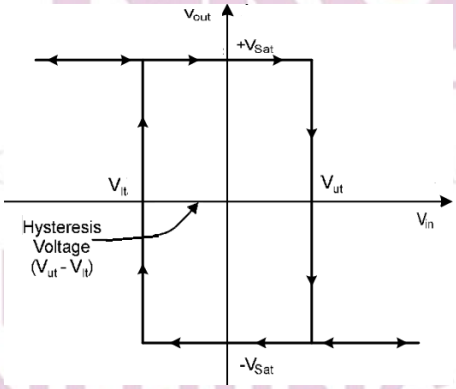
$$V_{hy} = \frac{R_1}{R_1 + R_2} \times [+V_{sat} - (-V_{sat})] \qquad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Input and output waveform for Schmitt trigger circuit is as shown in figure.



A graph of output voltage (V_O) versus input voltage (V_i) can be plotted for an invertingSchmitt Trigger Circuit Diagram, as shown in figure.

This input/output characteristic is called ***Hysteresis loop***.

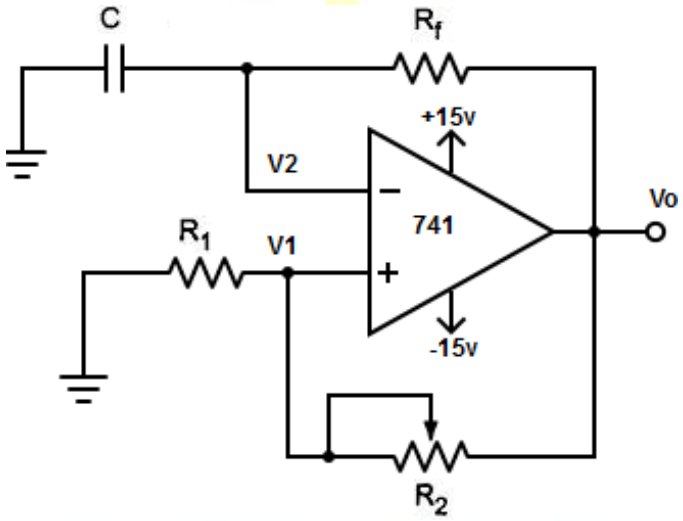


Explain Square wave generator circuit using Op. Amp.

The Square Wave Generator using Op Amp. means the Astable Multivibrator circuit using op-amp. It generates the square wave of required frequency. The figure shows thesquare wave generator using Op. Amp.

The circuit has a time dependent elements such as resistance and capacitor to set the frequency of oscillation.

As shown in the figure resistors R_1 and R_2 form an positive feedback.



When V_o is at $+V_{sat}$, the feedback voltage V_1 is called the upper threshold voltage V_{UT} and is given as

$$V_1 = V_{UT} = \frac{+V_{Sat}\, R_1}{R_1 + R_2} \quad \text{---- (1)}$$

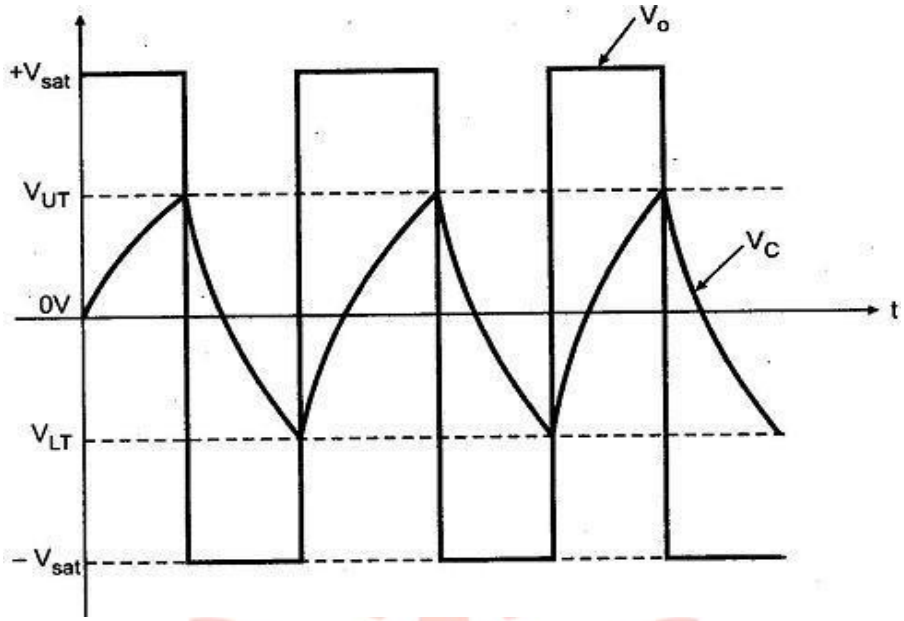
When V_o is at $-V_{sat}$, the feedback voltage V_1 is called the lower threshold voltage V_{LT} and is given as

$$V_1 = V_{LT} = \frac{-V_{Sat}\, R_1}{R_1 + R_2} \quad \text{---- (2)}$$

When power is turn ON, output is assumed to be $+V_{sat}$ because of positive feedback. With $V_o = +V_{sat}$ we have $V_1 = V_{UT}$ and capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f at the inverting input.

This is illustrated in figure. As long as the capacitor voltage V_c is less than V_{UT}, the output voltage remains at $+V_{sat}$

As soon as V_c charges to a value slightly greater than V_{UT}, the inverting (-) input becomes higher than non inverting (+) input. This switches the output voltage from +Vsat to -Vsat and we have $V_1 = V_{LT}$ which is negative with respect to ground. As V_o switches to $-V_{sat}$, capacitor starts discharging via **R_f,** as shown in the figure.



The current I discharges capacitor to 0 V and recharges capacitor to V_{LT}. When V_c becomes slightly more negative than the feedback voltage V_{LT}, the non inverting (+) input is higher than inverting (-) input. This switches the output voltage from -Vsat to
+Vsat and we have $V_1 = V_{UT}$ again which is positive with respect to ground..

As a result, capacitor now has a initial charge equal to V_{LT}. The capacitor will discharge from V_{LT} to O Volt and then recharge to V_{UT}, and the process is repeating. Once the, initial cycle is completed, the waveforms become periodic, as shown in the figure.

The frequency of oscillation is determined by the time it takes the capacitor to charge from V_{UT} to V_{LT} and vice versa.

Time period of output waveform is given by equation

$$T = 2RC\ ln\ [\frac{2R_1 + R_2}{R_2}] \quad \text{---- (3)}$$

Hence frequency of output waveform is given by equation

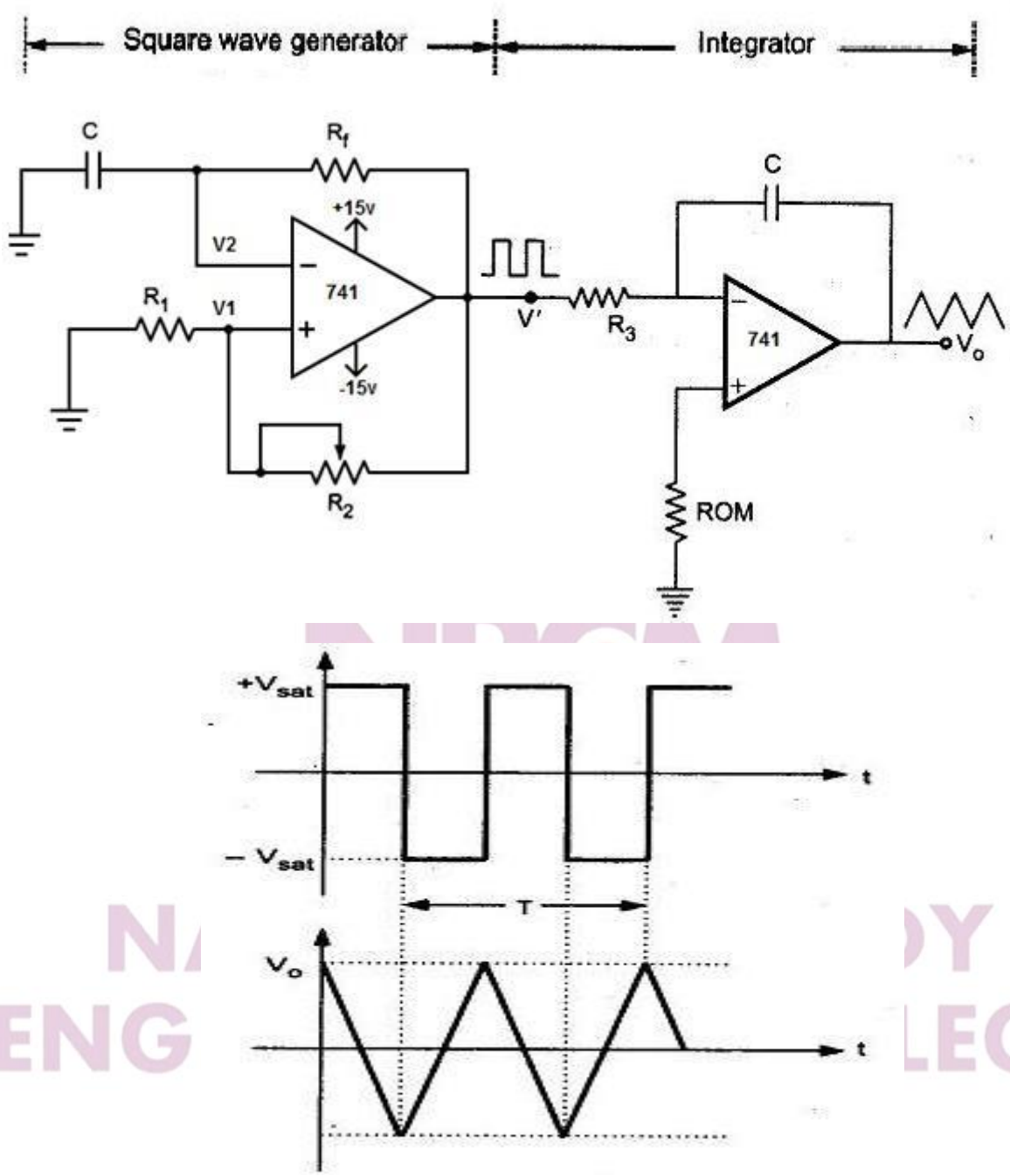
$$f = \frac{1}{T} = \frac{1}{2RC\ ln\ [\frac{2R1 + R2}{R_2}]} \quad \text{--- (4)}$$

in equation (4) if $R_2 = 1.16R_1$ then

$$f = \frac{1}{2RC} \quad \text{---- (5)}$$

Explain Triangular wave generator circuit using Op. Amp.

As we know that output of integrator is a Triangular Wave, if its input is a square wave. This means that a Triangular Wave Generator Using Op Amp can be formed by simply connecting an integrator to the square wave generator as shown in the figure.

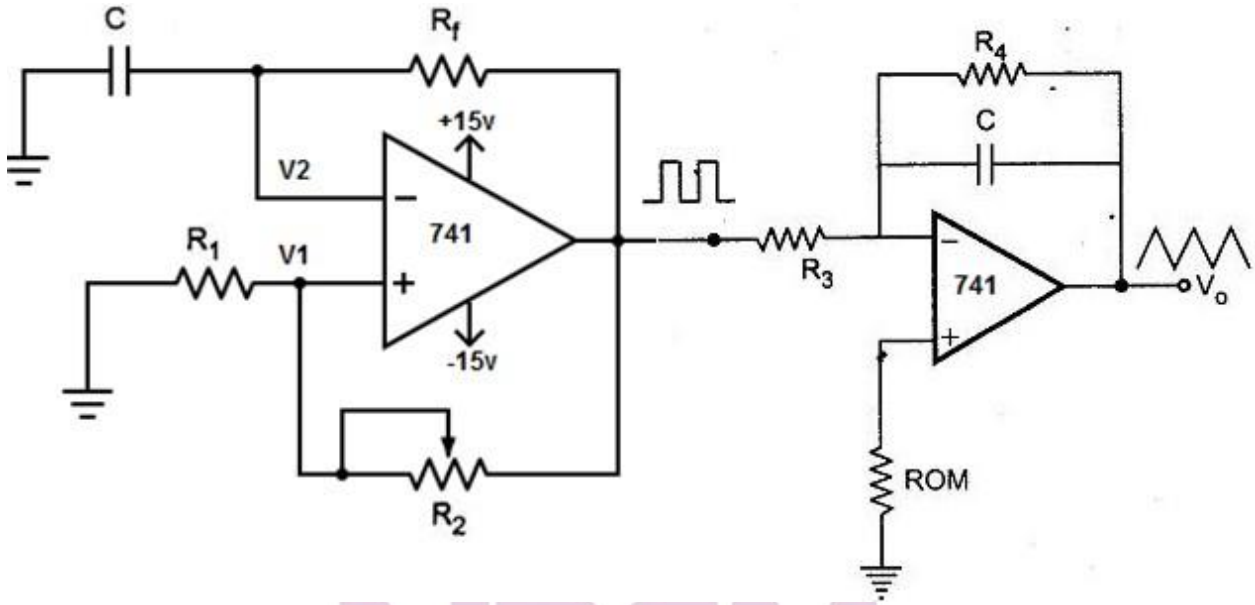


Basically, triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. This is achieved by connecting integrator circuit at the output of square wave generator. Assume that V' is high at $+V_{sat}$. This forces a constant current ($+V_{sat}/R_3$) through C (left to right) to drive V_o negative linearly. When V' is low at $-V_{sat}$, it forces a constant current ($-V_{sat}/R_3$) through C (right to left) to drive

V_o positive, linearly. The frequency of the triangular wave is same as that of square wave.

This is illustrated in figure. Although the amplitude of the square wave is constant ($\pm V_{sat}$), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa. This is because the reactance of capacitor decreases at high frequencies and increases at low frequencies.

In practical circuits, resistance R_4 is connected across C to avoid the saturation problem at low frequencies as in the case of practical integrator as shown in the figure.



Time period of output waveform is given by equation

$$T = 2RC\ ln\ [\frac{2R_1 + R_2}{R_2}] \quad \text{---- (1)}$$

Hence frequency of output waveform is given by equation

$$f = \frac{1}{T} = \frac{1}{2RC\ ln\ [\frac{2R1 + R2}{R_2}]} \quad \text{--- (2)}$$

in equation (4) if $R_2 = 1.16R_1$ then

$$f = \frac{1}{2RC} \quad \text{---- (3)}$$

Explain precision Half wave rectifier circuit using Op. Amp.

Rectifier circuits can be also implemented with a diode/diodes (half wave rectifier or full wave rectifier).

The major limitations of these Rectifiers circuits is that they cannot rectify voltages below $V_D = 0.7$ V, the cut-in voltage of the diode. Hence

$$V_o = V_i - V_{D(ON)} \quad \text{for } V_i \geq V_{D(ON)}$$

$$V_o = 0 \text{ V} \quad \text{for } V_i \leq V_{D(ON)}$$

Due to this, output of the conventional rectifier is distorted.

To achieve ***Precision Rectifiers*** we need a circuit that keeps V_o equal to V_i for $V_i > O$ V. This can be achieved by using Op. Amp. along with the diodes and these circuits are called ***Precision Rectifiers***. These are used to precisely rectify voltages having amplitudes less than 0.7 V.

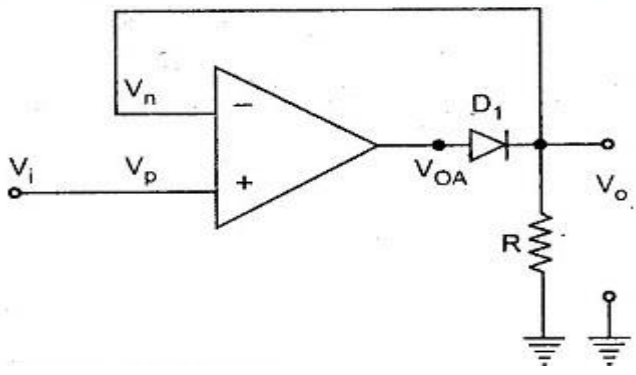
Precision Half Wave Rectifiers

There are two types of precision half wave rectifiers available,

(i) Non inverting half wave rectifier
(ii) Inverting half wave rectifier

Non inverting Half Wave Rectifier:

Figure shows precision half wave rectifier. It consists of non inverting amplifier with diode D_1 in the feedback loop of an Op. Amp



The analysis of this circuit can be done considering two distinct cases for$V_i > 0$ V

and $V_i < 0$ V

CASE 1 : $V_i > O$ V :

For closed loop Op. Amp. $V_p = V_n$, due to virtual ground.

When $V_i > 0$, Op. Amp. tries to keep $V_o = V_n = V_p = V_i$ (Voltage follower circuit) and it does this because forward biasing diode provides closed loop feedback path. The voltage drop across forward bias diode $V_D = 0.7$ V.

To accommodate the voltage drop across diode the Op. Amp. swings about 0.7 V higher than V_o, as shown in the figure.

CASE 2 : $V_i < O$ V :

When $V_i <$ O V, diode D_1 is reverse biased and the Op. Amp. is working in the open loop, as shown in the figure.

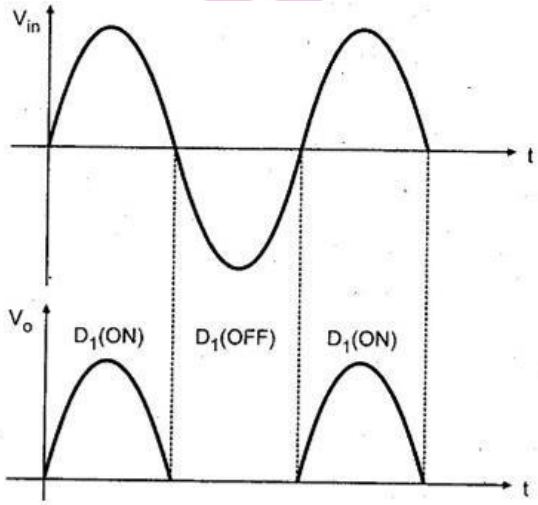
Therefore, Op. Amp. is no longer capable of keeping $V_n = V_p$. With no

current through resistance R we have $V_0 = 0$.

Since $V_n = V_o = 0$

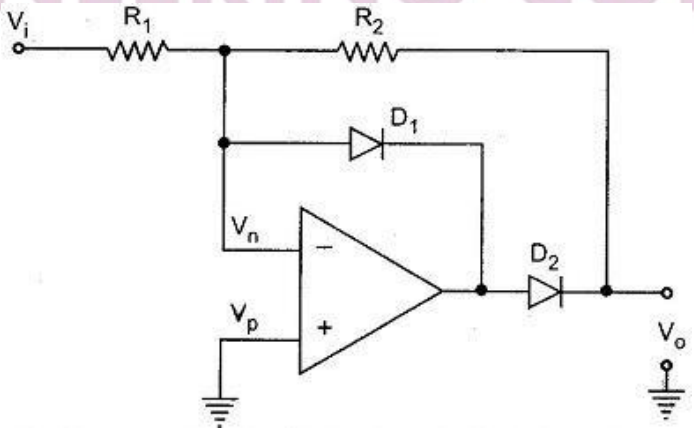
and $V_p = V_i < 0$,

The input and output waveforms are shown in figure



Inverting Half Wave Rectifier

Figure shows another popular circuit, inverting half-wave rectifier. It consists of two diodes and two resistors and Op. Amp. is connected in the inverting configuration.



CASE 1: $V_i > 0$:

Recalling virtual ground concept we can say that $V_p = V_n = O$ V.

For $V_i > 0$, V_i is positive with respect to V_n and hence current through R_1 flows from left to right. Only one path for this current to flow is through diode D_1. Hence diode D_1 is forward biased and diode D_2 is reverse biased. As current flow through R_2 is zero, $V_o = V_n = O$ V.

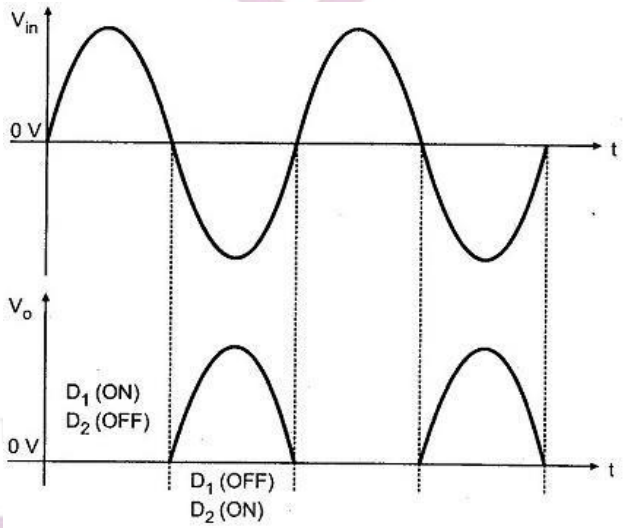
CASE 2 : $V_i < 0$:

For $V_i < 0$, V_i is negative with respect to V_n and hence current through R_1 flows from right to left. Only one path for this current to flow is through diode D_2 and resistor R_2, indicating that $V_0 > V_n$. Hence diode D_1 is OFF, and diode D_2 is ON. With these diode states, circuit acts like an inverting amplifier and output voltage is given as

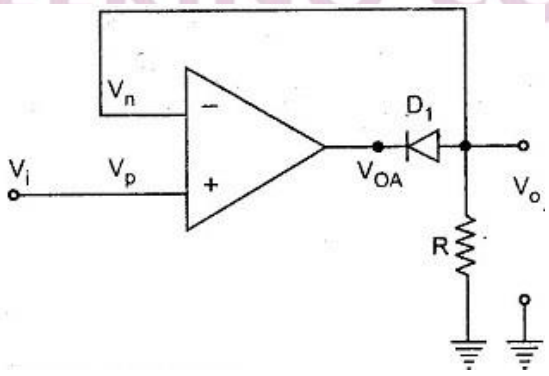
$$V_o = -\frac{R_2}{R_1} V_i \quad \text{for } V_i < 0 \text{ V}$$

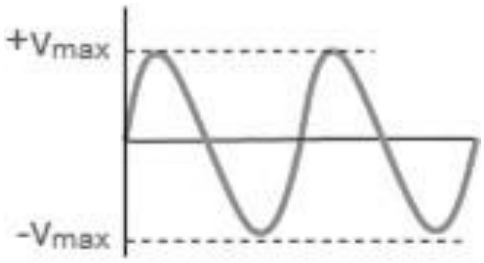
If R_1 and R_2 are made equal, then we can write $V_o = -V_i$The input

and output waveforms are shown in figure.

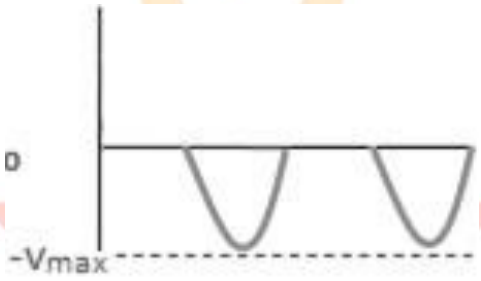


Non inverting Half Wave Rectifier which rectifies negative half cycle:



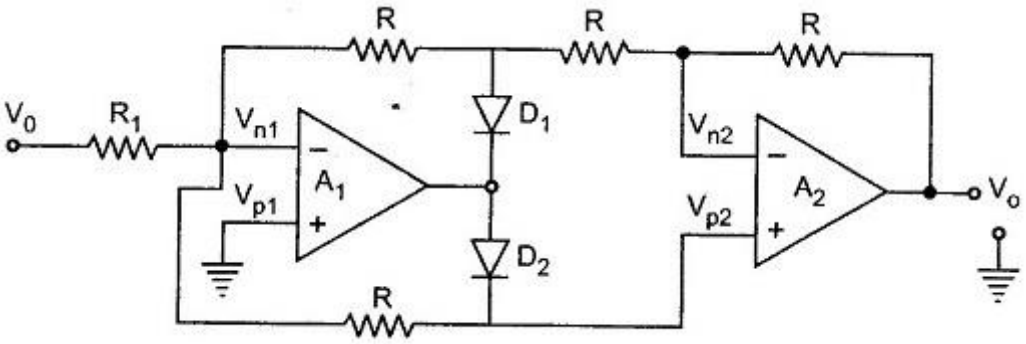


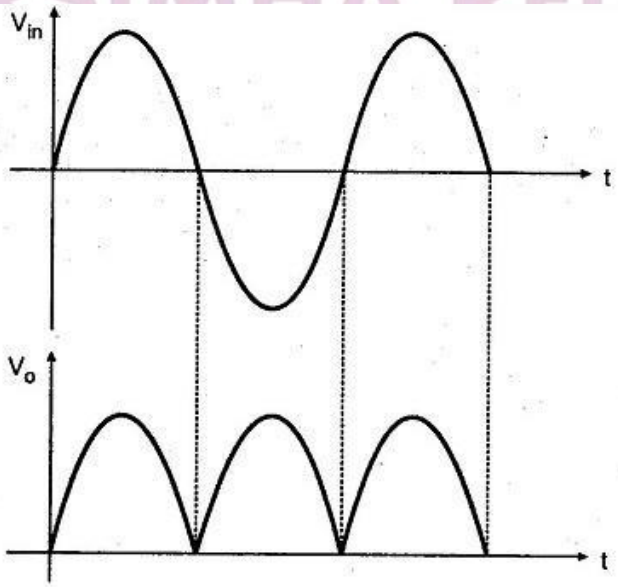
Input waveform



Output waveform

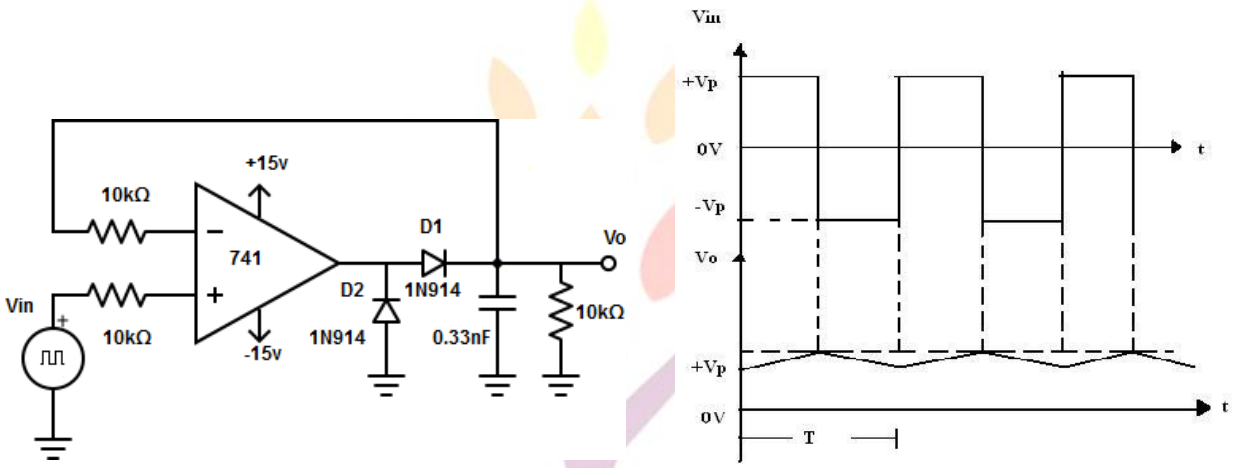
Precision Full Wave Rectifier:





Explain Peak Detector circuit using Op. Amp

Square, Triangular, Sawtooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional ac voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the RMS value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.



During the positive half cycle of V_{in}:

The output of the Op. Amp. drives D_1 in Forward bias, Charging capacitor C to thepositive peak value V_p of the input volt V_{in}.

During the negative half cycle of V_{in}:

D_1 is reverse biased and voltage across C is retained. The only discharge path forC is through R_L.

For proper operation of the circuit, the charging time constant (CR_d) and dischargingtime constant (CR_L) must satisfy the following condition.

$CR_d <= T/10$

Where R_d = Resistance of the forward-biased diode.T = time period of the input waveform.

$CR_L >= 10T$

Where R_L = Load Resistor.

Resistor R is used to protect the op-amp against the excessive discharge currents.
Diode D_2 conducts during the –ve half cycle of V_{in} and prevents the op-amp from goinginto negative saturation.

Negative peak of the input signal can be detected simply by reversing diode D_1 and D_2.

UNIT III

ACTIVE FILTERS AND OSCILLATOR

Filter

Filter is a frequency selective circuit that passes signal of specified Band of frequencies and attenuates the signals of frequencies outside the band

Type of Filter

1. Passive filters
2. Active filters

Passive filters

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation

Active filters

Active filters used op- amp as the active element and resistors and capacitors as passive elements. By enclosing a capacitor in the feed back loop , inductor less active filters can be obtained

Some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

Active Filters

• Active filters use op-amp(s) and RC components.

• Advantages over passive filters:

– op-amp(s) provide gain and overcome circuit losses

– increase input impedance to minimize circuit loading

– higher output power

– sharp cutoff characteristics can be produced simply and efficiently without bulky inductors

• Single-chip universal filters (e.g. switched-capacitor ones) are available that can be configured for any type of filter or response.

Review of Filter Types & Responses

• 4 major types of filters: low-pass, high-pass, band pass, and band-reject or band-stop

• 0 dB attenuation in the pass band (usually)

• 3 dB attenuation at the *critical* or *cutoff frequency*, f_c (for Butterworth filter)

• Roll-off at 20 dB/dec (or 6 dB/oct) per *pole* outside the passband (# of poles = # of reactive elements). Attenuation at any frequency, f, is

• Bandwidth of a filter: BW = f_{cu} - f_{cl}

• Phase shift: 45o/pole at f_c; 90o/pole at >> f_c

• 4 types of filter responses are commonly used:

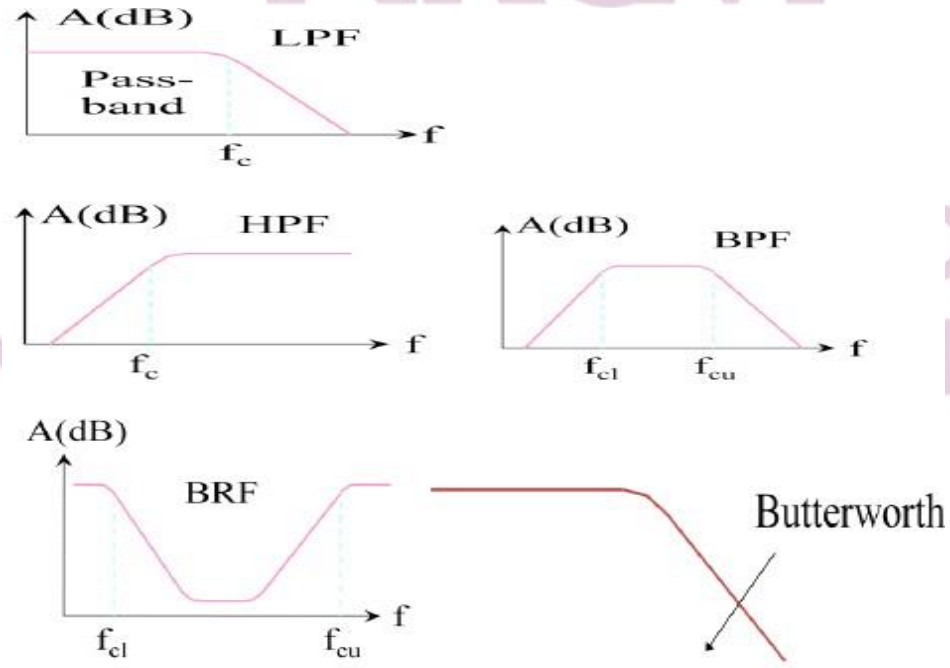
– Butterworth - maximally flat in passband; highly non-linear phase response with frequency

– Bessel - gentle roll-off; linear phase shift with freq.

– Chebyshev - steep initial roll-off with ripples in passband

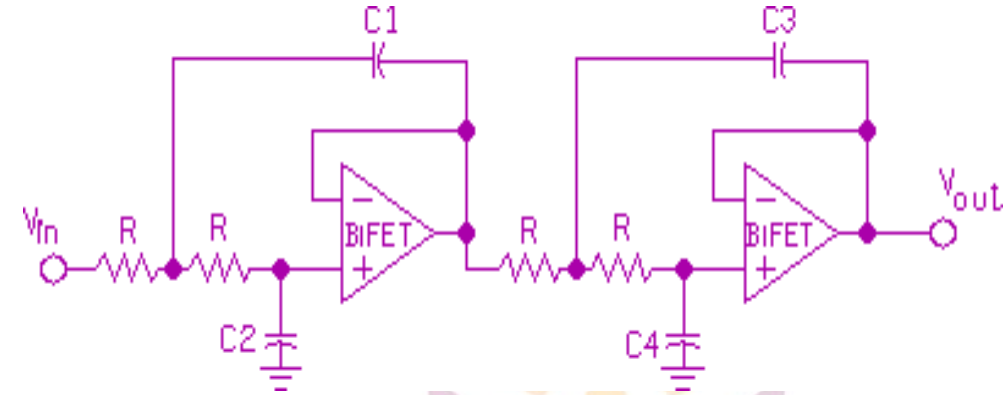
– Cauer (or elliptic) - steepest roll-off of the four types but has ripples in the passband and in the stop band

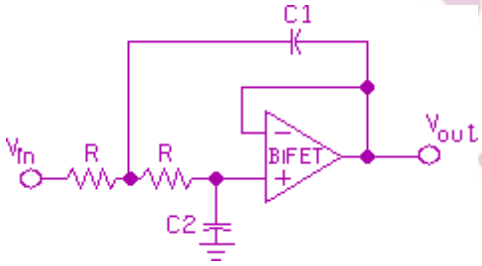
Frequency Response of Filters

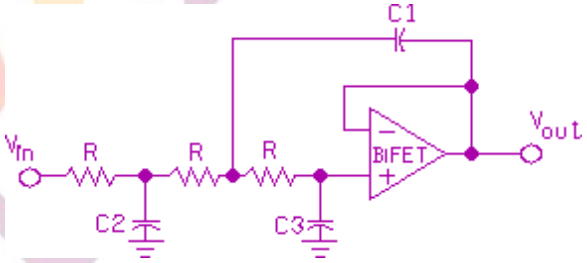


Unity-Gain Low-Pass Filter Circuits

Unity-Gain Low-Pass Filter Circuits







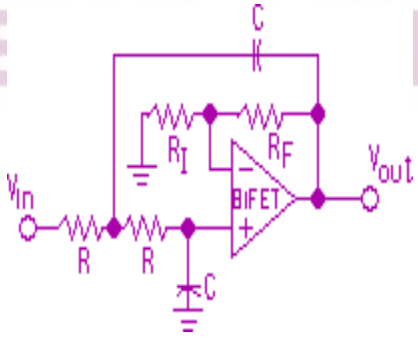
Design Procedure for Unity-Gain HPF

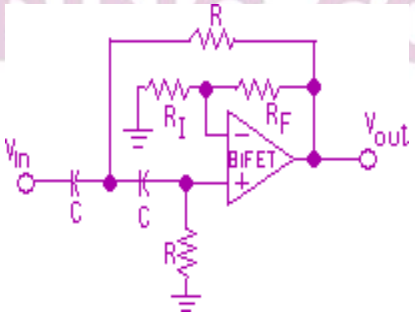
• The same procedure as for LP filters is used except for step #3, the normalized C value of 1 F is divided by K_f. Then pick a desired value for C, such as 0.001 mF to 0.1 mF, to calculate K_x. (Note that all capacitors have the same value).

• For step #6, multiply all normalized R values (from table) by K_x.

E.g. Design a unity-gain Butterworth HPF with a critical frequency of 1 kHz, and a roll-off of 55 dB/dec. (Ans.: C = 0.01 mF, R_1 = 4.49 kW, R_2 = 11.43 kW, R_3 = 78.64 kW.; pick standard values of 4.3 kW, 11 kW, and 75 kW).

Equal-Component Filter Design





Design an equal-component LPF with a critical frequency of 3 kHz and a roll-off of 20 dB/oct.

Minimum # of poles = 4

Choose C = 0.01 mF; ˆ R = 5.3 kW

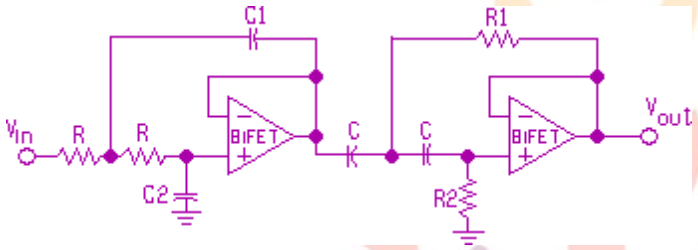
From table, A_{v1} = 1.1523, and A_{v2} = 2.2346.

Choose $R_{I1} = R_{I2}$ = 10 kW; then R_{F1} = 1.5 kW, and R_{F2} = 12.3 kW .

Select standard values: 5.1 kW, 1.5 kW, and 12 kW**.**

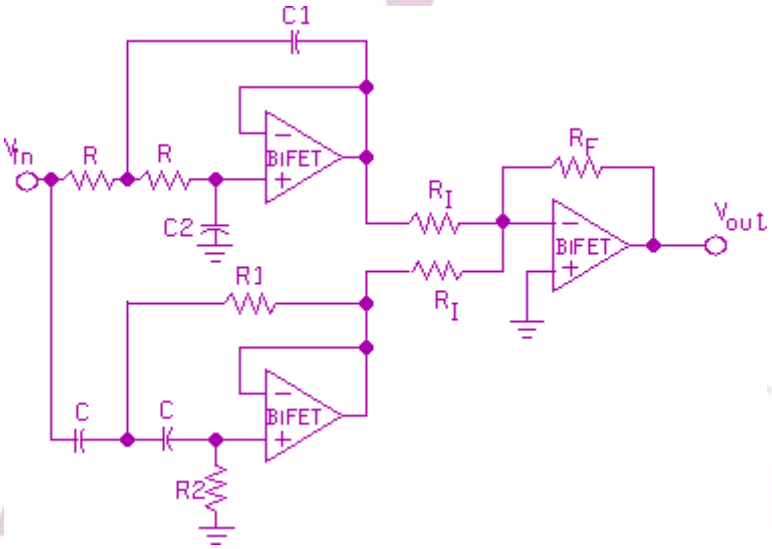
Bandpass and Band-Rejection Filter

A *broadband* BPF can be obtained by combining a LPF and a HPF

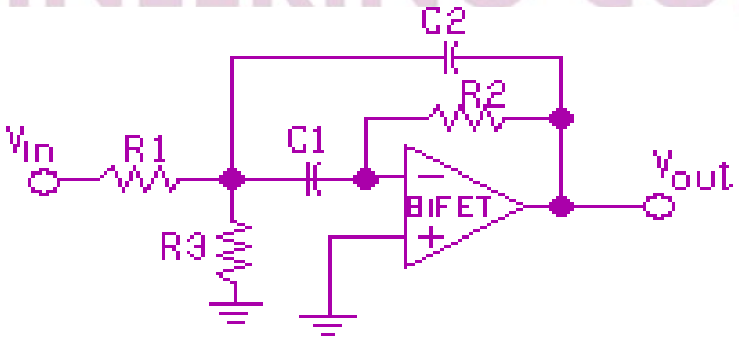


Broadband Band-Reject Filter

A LPF and a HPF can also be combined to give a broadband BRF

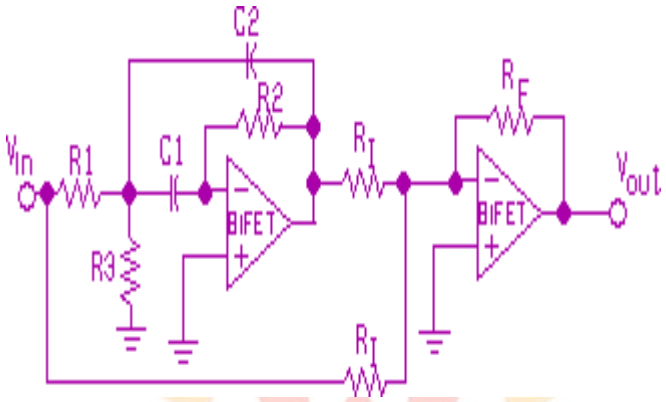


Narrow-band Bandpass Filter



Narrow-band Band-Reject Filter

Easily obtained by combining the inverting output of a narrow-band BRF and the original signal



The equations for R1, R2, R3, C1, and C2 are the same as before.

$R_I = R_F$ for unity gain and is often chosen to be >> R1.

Classification of ADCs

1. Direct type ADC.
2. Integrating type ADC

Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter

Integrating type converters

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter

Sample and hold circuit

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems

Dual slope ADC:

Dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator, and then measured by a counter. The speed of this conversion is slow but the accuracy is high

Advantages of dual slope ADC are

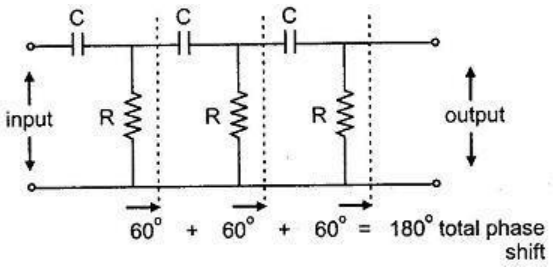
1. It is highly accurate
2. Its cost is low
3. It is immune to temperature caused variations in R1 and C1

Explain RC phase shift Oscillator using Op. Amp,

RC Phase Shift Oscillator basically consists of an amplifier and a feedback network consisting of resistors and capacitors arranged in ladder fashion. Hence such an oscillator is also called ladder type RC Phase Shift Oscillator.

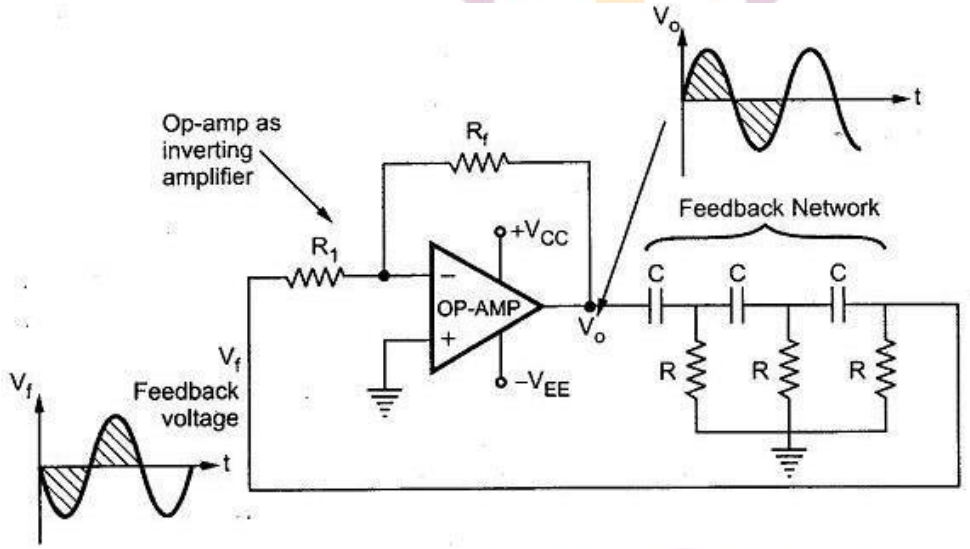
RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. Thus if one RC network produces phase shift of 60° then to produce phase shift of 180° such three RC networks must be connected in cascade.

Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60°, thus total phase shift due to feedback is 180° (3x 60°). Such a feedback network is shown in the figure.



The network is also called the **ladder network.** All the resistance values and all the capacitance values are same, so that for a particular frequency, each section of R and C produces a same phase shift of 60°.

In R-C phase shift oscillator op-amp connected in inverting amplifier mode. Thus itintroduces the phase shift of 180° between input and output. The feedback network consists of 3 RC sections each producing 60° phase shift. Hence total phase shift around a close loop is 360°. Such a RC phase shift oscillator using op-amp is shown in the figure.



The output of amplifier is given to feedback network. The Output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$f = \frac{1}{2\pi\sqrt{6}\,RC}$$

The frequency is measured in Hz.

At this frequency the gain of the op-amp must be at least 29 to satisfy loop gain Aβ = 1. Now gain of the op-amp inverting amplifier is given by,

$$|A| \geq \frac{R_f}{R_1} \geq 29 \text{ for oscillations}$$

$$R_f \geq 29\, R_1$$

Thus circuit will work as an oscillator which will produce a sinusoidal waveform if gain is 29 and total phase shift around a loop is 360°. This satisfies the Barkhausen criterion for the oscillator. These oscillators are used over the audio frequency range i.e. about 20Hz up to 100 kHz.

Advantages

(i) The circuit is simple to design.

(ii) Can produce output over audio frequency range.

(iii) Produces sinusoidal output waveform.

(iv) It is a fixed frequency oscillator.

Disadvantages

(i) phase shift oscillator is fixed frequency oscillator. Frequency cannot be varied.

(ii) Frequency stability is poor.

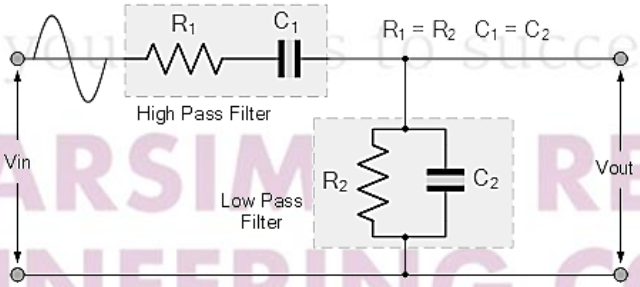
Explain Wien Bridge Oscillator using Op. Amp,

The Wien Bridge is one of the simplest and best known oscillators and is usedextensively in circuits for audio applications.

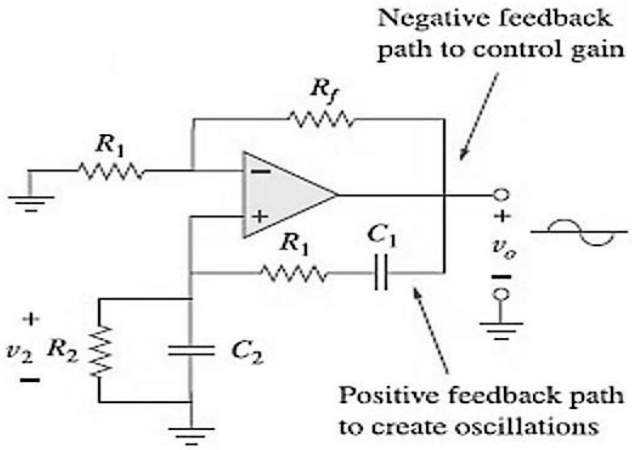
This is also RC oscillator which uses RC type of feedback network. Wien bridge oscillator uses a **non-inverting amplifier.** So in Wien bridge type there is no phaseshift necessary through the feedback network.

The two arms of the bridge, namely R1**,** C1 in series and R2, C2 in parallel are called **frequency sensitive arms.** This is because the components of these two arms decide the frequency of the oscillator.

Such a feedback network is called **lead–lag network.** .



The resistance R and capacitor C are the components of frequency sensitive arms of thebridge.



The resistance Rf and R1 form the part of the feedback path. The gain of non inverting op-amp can be adjusted using the resistance Rf and R1. The gain of op-amp is,

$$A = 1 + \frac{R_f}{R_1}$$

To satisfy Barkhausen criterion that AB=1 it is necessary that the gain of the non inverting op-amp amplifier must be minimum 3.

$$|A| \geq 3 \quad \text{i.e} \quad 1 + \frac{R_f}{R_1} \geq 3$$

$$\frac{R_f}{R_1} \geq 2$$

Thus ratio of Rf and R1 must be greater than or equal to 2.The frequency of oscillations is given by,

$$f = \frac{1}{2\pi RC} \text{ Hz}$$

The feedback is given to the non inverting terminal of op-amp which ensures zerophase shift.

If in a Wien bridge feedback network, two resistances are not equal i.e. they are R1 and R2 while two capacitors are not equal i.e. they are C1 and C2 then the frequency of oscillations is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

With $R_1 = R_2 = R$ and $C_1 = C_2 = C$ we get it as $1/2\pi RC$ as stated earlier.

Advantages

(i) It is stable.

(ii) We can change the frequency very effectively.

(iii) The perfect sine wave output is possible.

(iv) It is useful audio frequency range i.e. 20 Hz to 100 kHz.

Disadvantages

(i) The maximum frequency output is limited.

Explain Active Filters

Active Filters is a circuit that is designed to pass a specified band frequencies while attenuating all the signals outside that band. It is a frequency selective circuit.

The filters are basically classified as ***active filters*** and ***passive filters***. The passive filter networks use only passive elements such as resistors, inductors and capacitors. On the other hand, ***active filter circuits use the active elements such as op-amps, transistors along with the resistors, inductors and capacitors***. Modern active filters do not use inductors as the inductors are bulky, heavy and nonlinear. The inductors generate the stray magnetic fields. The inductors dissipate considerable amount of power.

Advantages of Active Filters

(i) **Flexibility in Gain and Frequency Adjustment :** The op-amp gain can be easily controlled in closed loop fashion, hence active filter input signal is not attenuated. The passive filters need the attenuation. The active filters can be easily tuned.

(ii) **No Loading Effect :** The op-amp has high input impedance and low output impedance. Hence active filter using op-amp does not cause loading of the source or load.

(iii) **Cost :** Due to availability of modern ICs, a variety of cheaper op-amps are available. The inductors are absent which makes the modern active filters more economical than passive filters.

The most commonly used filters are:

1) Low Pass (LP) filter

2) High pass (HP) filter

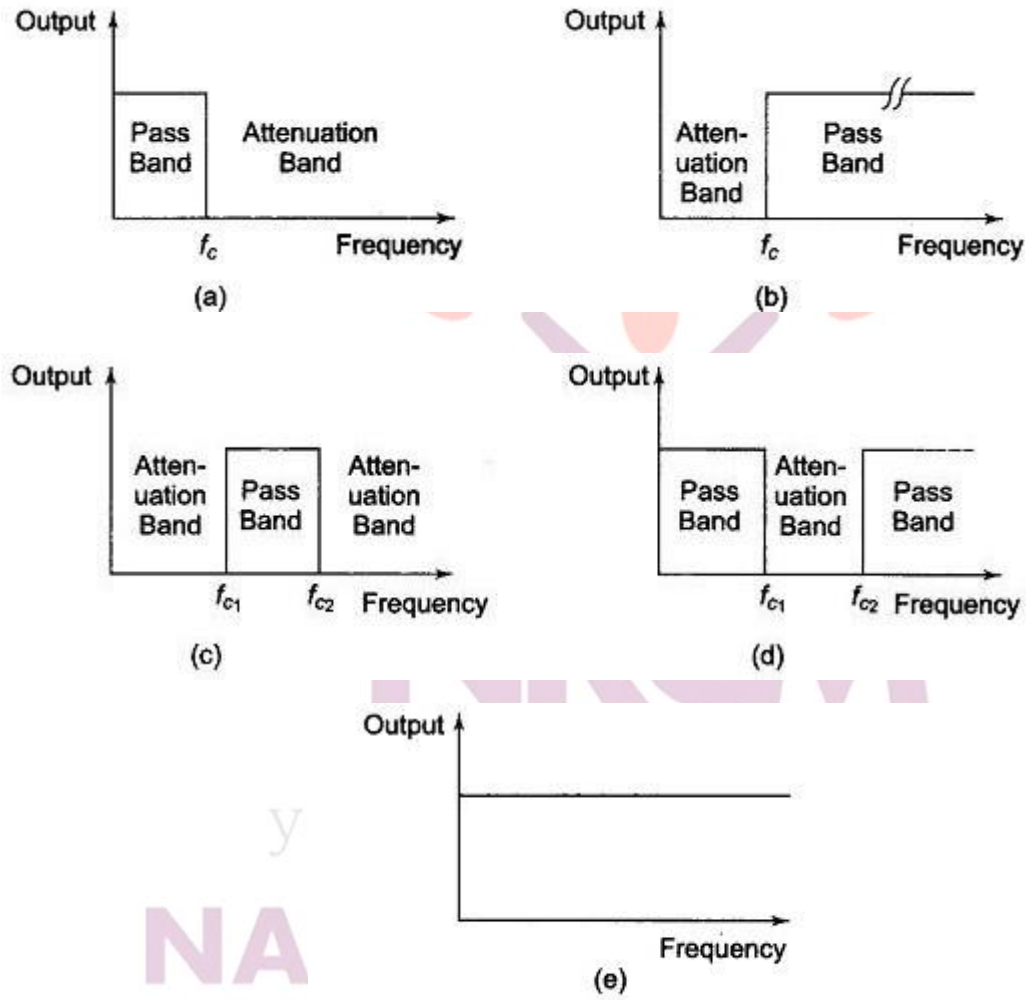
3) Band Pass (BP) filter

4) Band Reject (BR) filter. This is also called as Band Stop Filter (BS) or Band Elimination (BE) filter.

5) All Pass filter

Frequency response of Ideal filter:

Each of these filters use op-amp as an active element and resistors and capacitors.Frequency response characteristics of these types of filters are as follow:



Ideal Response of Various Filters (a) Low Pass (b) High Pass (c) Band Pass (d) Band Stop (e) All Pass

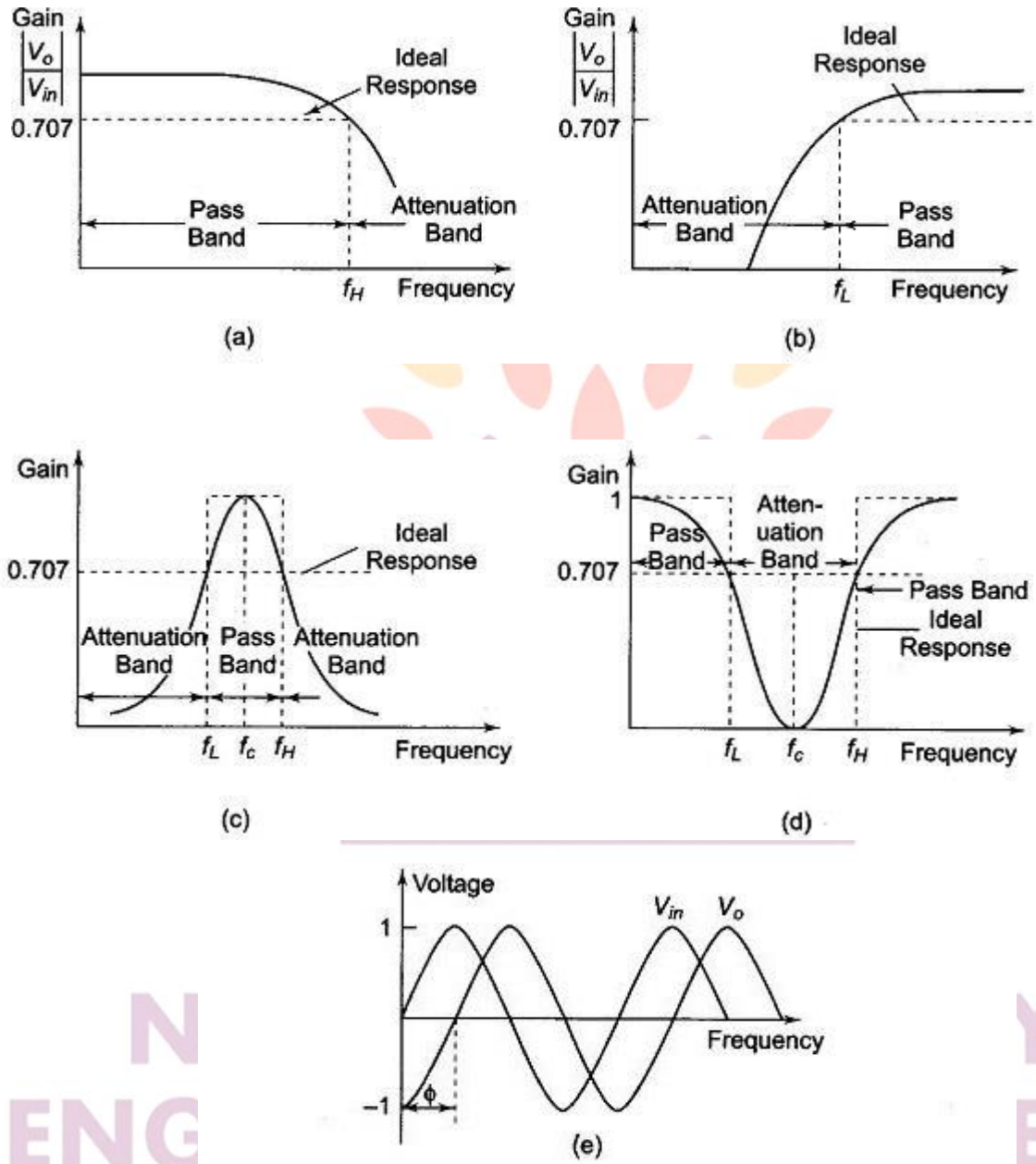
Active Filters Types:

There are basically four useful Active Filters Types.

1. Butterworth
2. Chebyschev
3. Bessel
4. Elliptic

Frequency response of major practical Active Filters

Figure shows the frequency response characteristics of the Active Filters Classification. The ideal response is shown by the dashed lines, while solid lines indicate the ***practical filter response.***



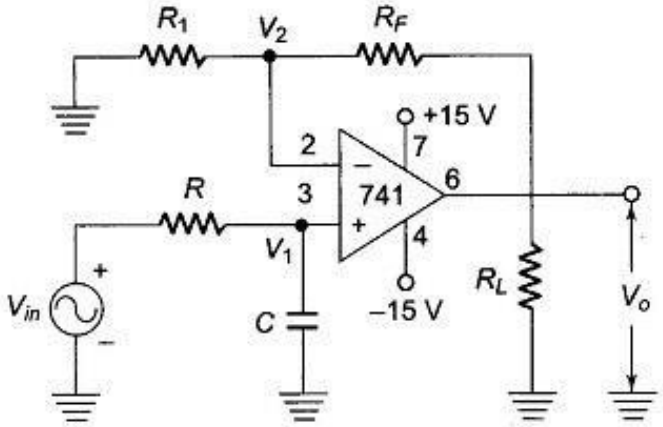
Frequency Response of Major Active Filters (a) Low Pass Filter (b) High Pass Filter (c) Band Pass Filter (d) Band Stop Filter (e) Phase Relation of Input and Output Waveform in an all Pass Filter

First order Law Pass Butterworth Filters

The Butterworth filter has an essentially flat amplitude versus frequency response upto the cutoff frequency.

A ***first order low pass Butterworth filter*** can be obtained from the Basic Low Pass Filter Circuit using an RC filter network.

Figure shows a first order low pass Butterworth filter that uses an RC network for filtering. The op.amp. is used in the non-inverting configuration, which does not load the RC network. R_1 and R_F determine the gain of the filter (in this case unity).



Using the voltage divider rule, the voltage across the capacitor, i.e. at the non-inverting input is

$$V_1 = \frac{-jX_c}{R - jX_c} \times V_{in}, \text{ but } -jX_c = \frac{1}{j2\pi f_C}$$

Simplifying, we get

$$V_1 = \frac{V_{in}}{j2\pi f CR + 1}$$

As output voltage

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \times V_1$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \times \left(\frac{V_{in}}{1 + j2\pi f CR}\right)$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j2\pi f RC} \text{ But } f_H = \frac{1}{2\pi RC}$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j(f/f_H)}$$

where

V_o/V_{in} = Gain of the filter as a function of frequency AF =

$1 + R_F/R_1$ = pass band gain of the filter

f= frequency of the input signal

$f_H = 1/2\,\pi\,RC$ = high cutoff frequency

The gain magnitude and phase angle can be obtained by applying modulus to

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^2}}$$

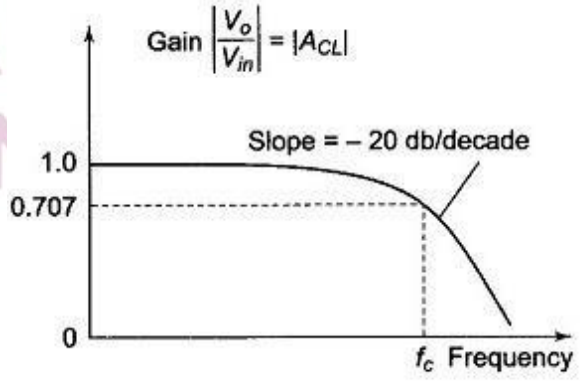
$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right)$$

where Φ is the phase angle in degrees.

The operation of the Basic Low Pass Filter Circuit can be verified from the gainmagnitude

1. At very low frequency, that is $f < f_H$,
$$\frac{V_o}{V_{in}} \cong A_F$$
2. At $f = f_H$, $\frac{V_o}{V_{in}} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$
3. At $f > f_H$, $\frac{V_o}{V_{in}} < A_F$

Hence the Basic Low Pass Filter Circuit has a constant gain, A_F, from 0 Hz to the high cutoff frequency f_H. At f_H, the gain is 0.707 A_F and after f_H the gain decreases at a constant rate with increase in frequency; when the frequency is increased 10 times(one decade), the voltage gain is divided by 10. In other words, the gain decreases by 20 db (20 log 10) each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20 db/decade or 6 db/octave, where octave signifies a two fold increase in frequency. The frequency $f = f_H$ is called the cutoff frequency.



.8 Low Pass Active Filter Frequency Response for a Roll off of – 20db/decade

The procedure of converting a cutoff frequency to a new cutoff frequency is called frequency scaling.

To obtain a new cutoff frequency, R or C (but not both) is multiplied by the ratio of the original cutoff frequency to the new cutoff frequency.

In filter design, the values required for R and C are often not standard, and a variable capacitor C is not commonly used. Hence, we choose a standard value of the capacitor and then calculate the value of the resistor required for a desired cutoff frequency. This is because for a non-standing value of a resistor, a potentiometer can be used.

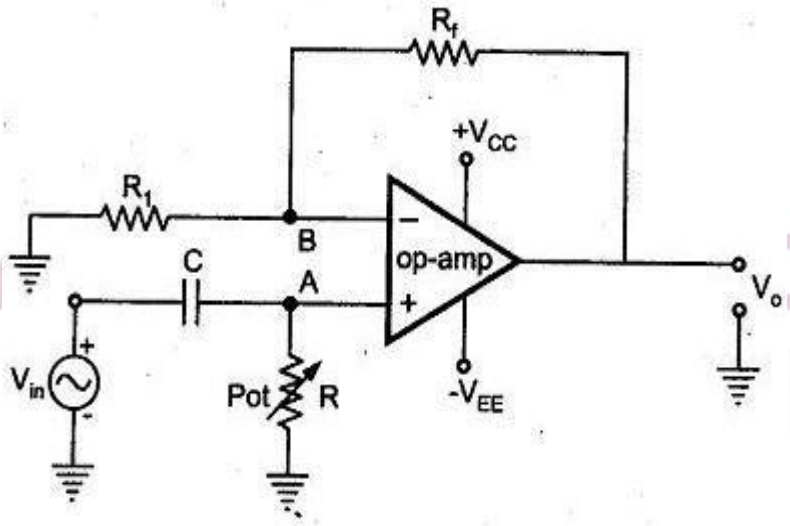
First order High Pass Butterworth Filters

The Butterworth filter has an essentially flat amplitude versus frequency response upto the cutoff frequency.

A ***first order high pass Butterworth filter*** can be obtained from the Basic high Pass Filter Circuit using an RC filter network.

Figure shows a first order high pass Butterworth filter that uses an RC network for filtering. The op.amp. is used in the non-inverting configuration, which does not load the RC network. R_1 and R_F determine the gain of the filter (in this case unity).

a high pass filter is a circuit that attenuates all the signals below a specified cut off frequency denoted as f_L. Thus, a high pass filter performs the opposite function to that of low pass filter. Hence, the First Order High Pass Butterworth Filter circuit can be obtained by interchanging frequency determining resistances and capacitors in low pass filter circuit.



The first order high pass filter can be obtained by interchanging the elements R and C in a first order low pass filter circuit. The figure shows the first order high pass Butterworth filter.

It can be observed that as compared to first order low pass filter, the positions of R and C are changed in the high pass circuit shown in figure.

The frequency at which the gain is 0.707 times the gain of filter in pass band (maximum) is called as low cut off frequency, and denoted as f_L. So, all the frequencies greater than f_L are allowed to pass but the maximum frequency which is allowed to pass is determined by the closed loop bandwidth of the op.amp. used.

Analysis of the Filter Circuit

The impedance of the capacitor is

$$-jX_C = -j\left(\frac{1}{2\pi fC}\right)$$

where f is the input i.e. operating frequency.

By the voltage divider rule, the potential of the non inverting terminal of the op.amp. is

$$V_A = V_{in}\left[\frac{R}{R - jX_C}\right]$$

$$V_A = V_{in}\left[\frac{R}{-jX_C\left(\frac{R}{-jX_C} + 1\right)}\right] \qquad \text{taking } -jX_C \text{ outside}$$

$$-\frac{1}{j} = j, \text{ we can write,}$$

$$\frac{1}{-jX_C} = \frac{j}{X_C} = \frac{j}{\left(\frac{1}{2\pi fC}\right)}$$

$$= j2\pi fC$$

Substituting in the above expression of V_A,

$$V_A = V_{in}\left[\frac{\left(-\frac{R}{jX_C}\right)}{\left(-\frac{R}{jX_C}\right) + 1}\right]$$

$$V_A = V_{in}\left[\frac{j2\pi fRC}{1 + j2\pi fRC}\right]$$

This can be represented as

$$\therefore \quad V_A = V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right]$$

where $f_L = \frac{1}{2\pi RC}$ = low cut off frequency

Now, for the op-amp in non-inverting configuration,

$$V_o = A_F V_A$$

where V_A = Voltage at the non inverting input

and $A_F = \left(1 + \frac{R_f}{R_1}\right)$ = gain of op–amp in pass band

$$\therefore \quad V_o = A_F V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right]$$

Hence,

$$\frac{V_o}{V_{in}} = A_F\left[\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right]$$

This is the required expression for the transfer function of the filter. For the frequencyresponse, we require the magnitude of the transfer function which is given by,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}}$$

1) At low frequencies, i.e. $f < f_L$

$$\left|\frac{V_0}{V_{in}}\right| < A_F$$

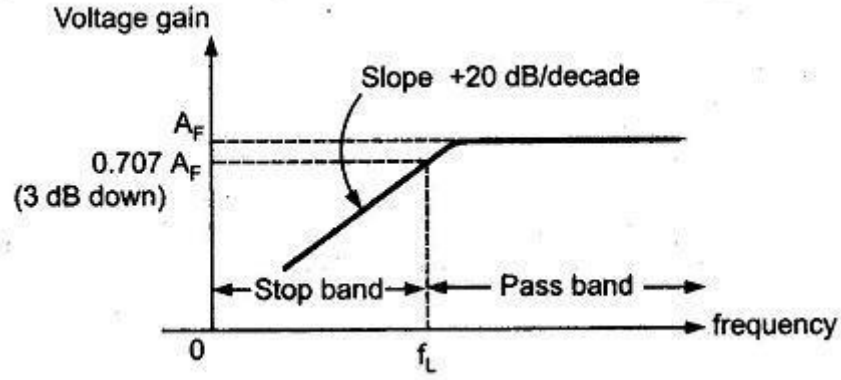
2) At $f = f_L$,

$$\left|\frac{V_0}{V_{in}}\right| = 0.707\ A_F$$ i.e. 3 dB down from the level of A_F

3) At $f > f_L$, i.e. high frequencies, 1 can be neglected as compared to $\left(\frac{f}{f_L}\right)$ from denominator.

$$\left|\frac{V_0}{V_{in}}\right| \cong A_F$$ i.e. constant

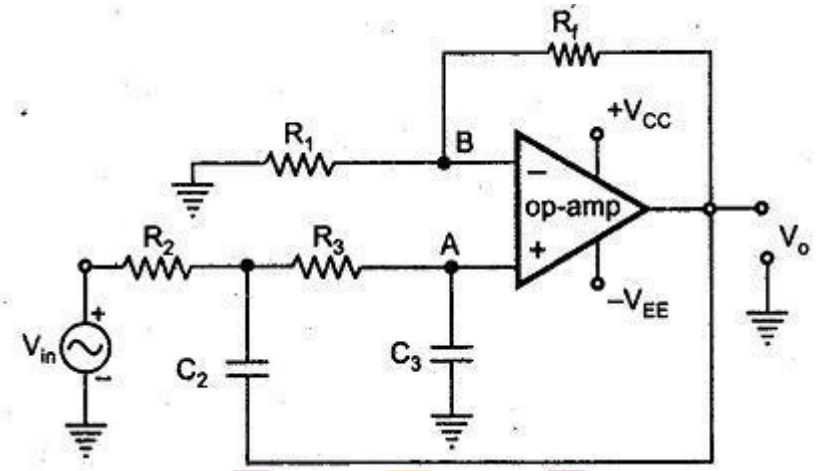
Thus, the circuit acts as high pass filter with a pass band gain as A_f. For the frequencies, $f < f_L$, the gain increases till $f = f_L$ at a rate of + 20 dB/decade. Hence, the slope of the frequency response in stop band is + 20 dB/decade for first order high pass filter. The frequency response is shown in the figure.



Note : As high pass filter is basically a low pass filter circuit with positions of R and C interchanged, the design steps and the frequency scaling method discussed earlier for low pass filter is equally applicable to the first order high pass Butterworth filter.

Second order Low Pass Butterworth Filters

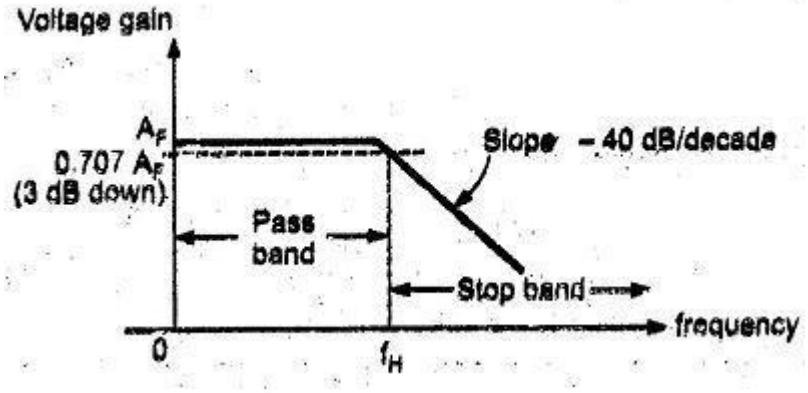
The practical response of Second Order Low Pass Butterworth Filter must be very close to an ideal one. In case of low pass filter, it is always desirable that the gain rolls off very fast after the cut off frequency, in the stop band. In case of first order filter, it rolls off at a rate of 20 dB/decade. In case of second order filter, the gain rolls off at a rate of 40 dB/decade. Thus, the slope of the frequency response after $f = f_H$ is -40 dB/decade, for a second order low pass filter.



A first order filter can be converted to second order type by using an additional RC network as shown in the figure.

The cut off frequency f_H for the filter is now decided by R_2, C_2, R_3 and C_3. The gain of the filter is as usual decided by op-amp i.e. the resistance R_1 and R_f.

The frequency response is shown in figure.

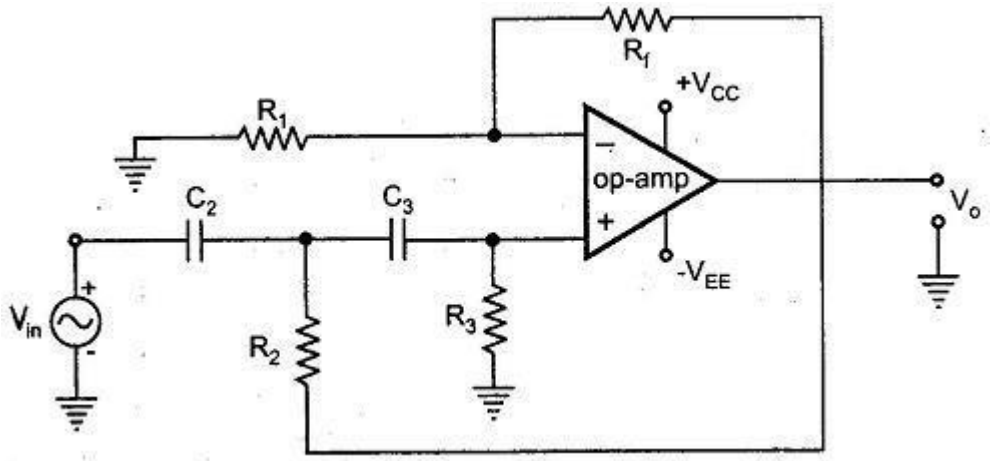


At the cut off frequency f_H, the gain is 0,707 A_f i,e. 3 dB down from its 0 Hz level. After, f_H ($f > f_H$) the gain rolls off at a frequency rate of 40 dB/decade,. Hence, the slope of the 'response after, f_H is – 40 dB/decade.

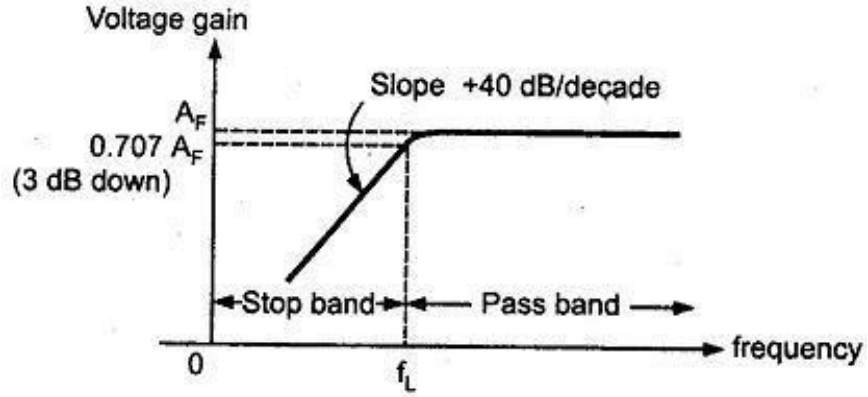
Second order Low Pass Butterworth Filters

The second order high pass Butterworth filter produces a gain roll off at the rate of + 40dB/decade in the stop band. This filter also can be realized by interchanging the positions of resistors and capacitors in a second order low pass Butterworth filter. The figure shows the second order high pass Butterworth filter.

The analysis, design and the scaling procedures for this filter is exactly same as that of second order low pass Butterworth filter.



The frequency response of this filter is shown in the figure.



UNIT IV

TIMERS AND PHASE LOCKED LOOPS

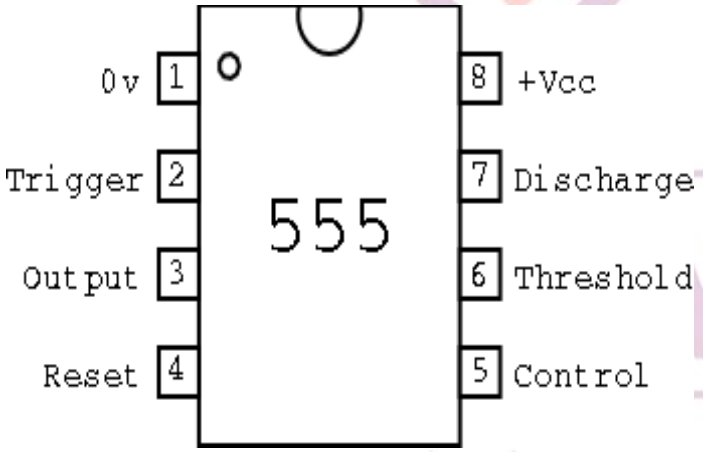
555 Timer:

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions. IC NE/SE 555 is a highly stable device for generating accurate time delays. Commercially, this IC is available in 8-pin circular, TO-99 or 8-pin DIP or 14-pin DIP packages.

The salient features of 555 Timer IC's are:

- ✓ Compatible with both TTL and CMOS logic families.
- ✓ The maximum load current can go up to 200 mA.
- ✓ The typical power supply is from +5V to +18 V
- ✓

Pin diagram of 555 timer is as shown in figure:



Features of 555 Timer Basic blocks

1. It has two basic operating modes: monostable and astable
2. It is available in three packages. 8 pin metal can , 8 pin dip, 14 pin dip.
3. It has very high temperature stability

Applications of 555 Timer

1. astable multivibrator
2. monostable multivibrator
3. Missing pulse detector
4. Linear ramp generator

5. Frequency divider
6. Pulse width modulation
7. FSK generator
8. Pulse position modulator
9. Schmitt trigger

Multivibrator

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator

Monostable multivibrator

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi- stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state

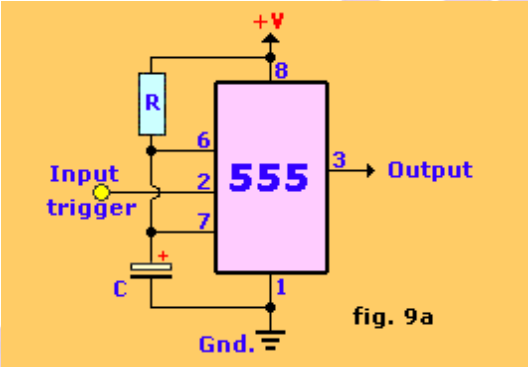
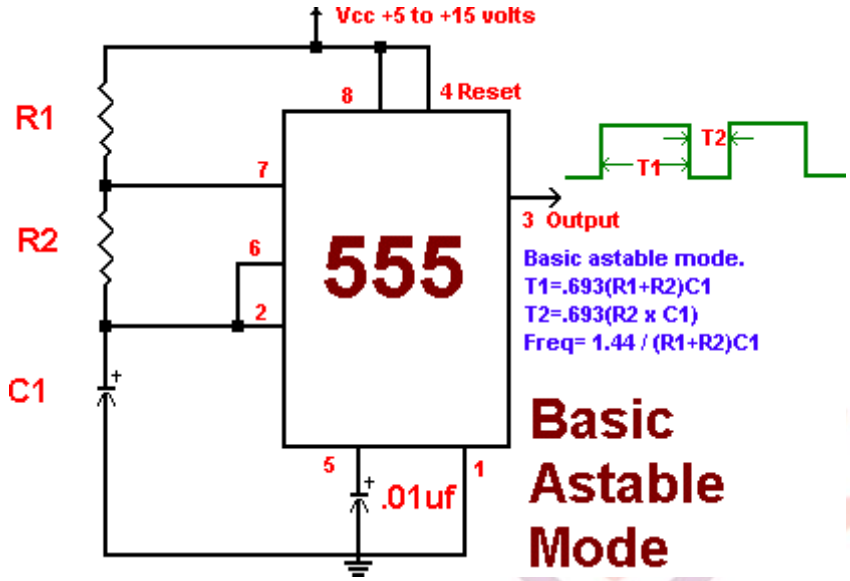


fig. 9a

Astable multivibrator

Astable multivibrator is a free running oscillator having two quasi- stable states. Thus, there is oscillations between these two states and no external signal are required to produce the in state Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state,

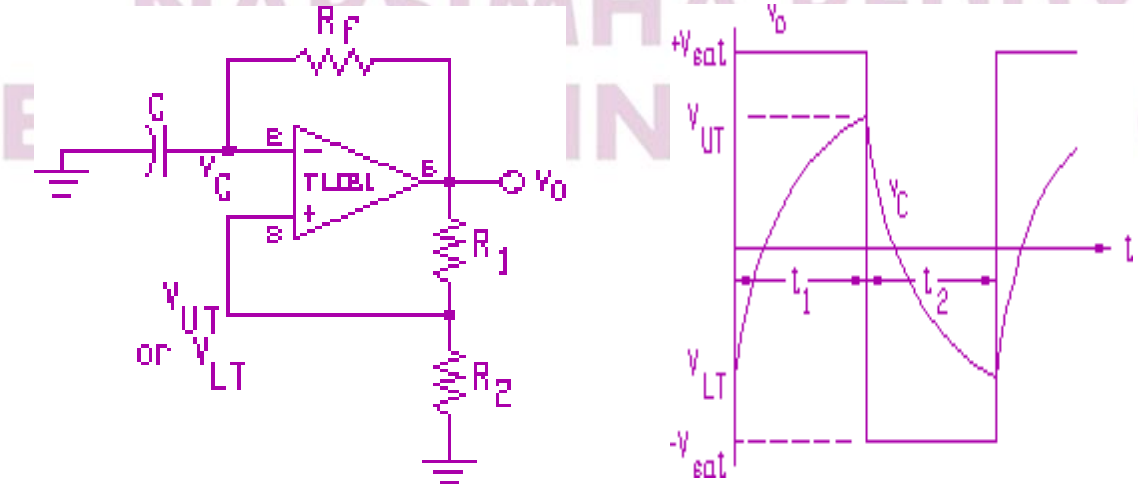
and this output level is maintained indefinitely until an second trigger is applied. Thus, it requires two external triggers before it returns to its initial state



Bistable multivibrator

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied. Thus, it requires two external triggers before it returns to its initial state

Astable Multivibrator or Relaxation Oscillator



4.5.1 Equations for Astable Multivibrator

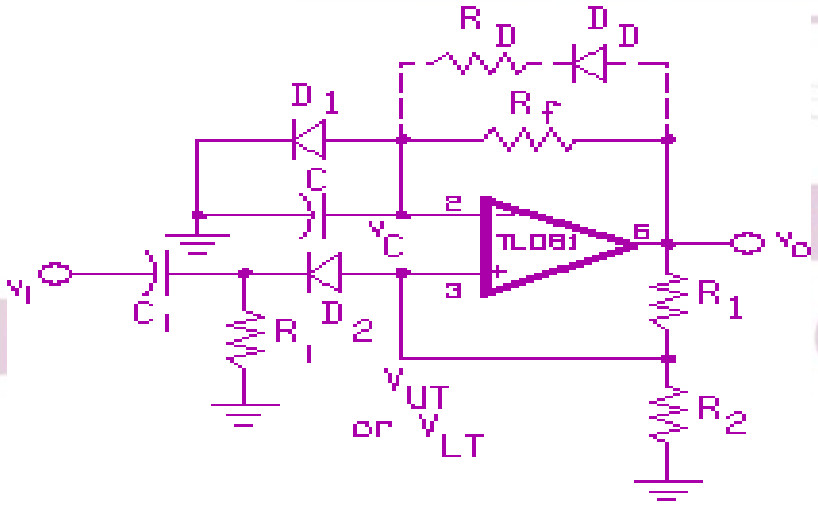
$$V_{UT} = \frac{+V_{sat}R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat}R_2}{R_1 + R_2}$$

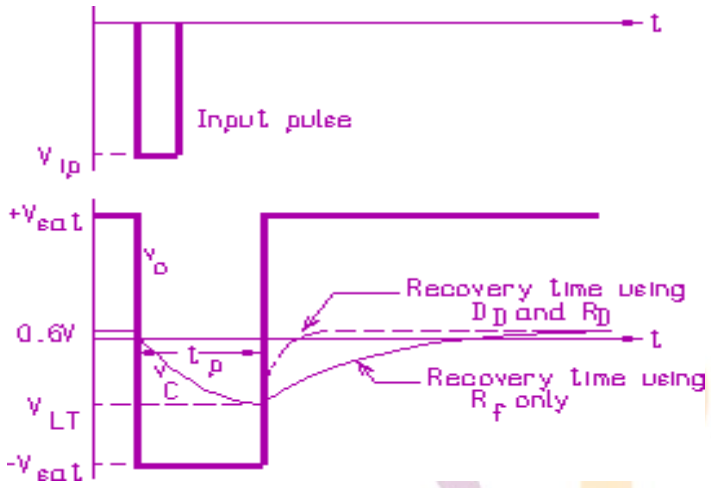
$$V_{UT} = \frac{+V_{sat}R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat}R_2}{R_1 + R_2}$$

$$T = t_1 + t_2 = 2\tau \ln\left(\frac{R_1 + 2R_2}{R_1}\right)$$

$$f = \frac{1}{2R_fC}$$

Monostable (One-Shot) Multivibrator





4.6.1 Notes on Monostable Multivibrator:

• Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V

• Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select $R_iC_i \# 0.1R_fC$.

• Timing state: C charges negatively from 0.6 V through R_f. Width of timing pulse is:Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V

• Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select $R_iC_i \# 0.1R_fC$. Timing state: C charges negatively from 0.6 V through R_f.

Recovery state: $v_o = +V_{sat}$; circuit is not ready for retriggering until $V_C = 0.6$ V. The *recovery time* t_p. To speed up the recovery time, R_D (= $0.1R_f$) & C_D can be added.

Voltage controlled oscillator

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage

4.7.1 The features of 566 VCO

1. Wide supply voltage range(10- 24V)
2. Very linear modulation characteristics
3. High temperature stability

Phase Lock Looped

A PLL is a basically a closed loop system designed to lock output frequency and phase to the frequency and phase of an input signal

4.8.1 Applications of 565 PLL

1. Frequency multiplier
2. Frequency synthesizer
3. FM detector

UNIT V

D-A and A-D Convereter

Introduction

- Digital-to-analog (D/A) and analog-to-digital (A/D) converters constitute an essential link when digital devices interface with analog devices, and vice versa. They are important building blocks of any digital system, including both communication and non-communication systems, besides having other applications.

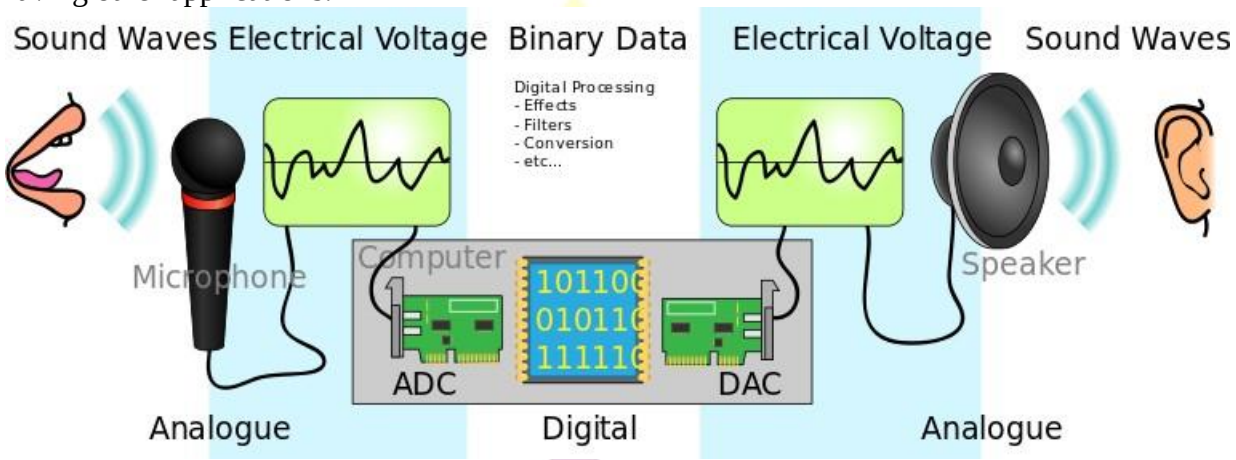


Fig.: Illustration of ADC and DAC

Digital to Analog Converter (D/A Converter)

- For the results of digital computations to be used in the analog world, it becomes necessary to convert the digital values to proportional analog values.
- Unlike analog signals, digital data can be transmitted, manipulated, and stored without degradation. But a DAC is needed to convert the digital signal to analog to drive an earphone or loudspeaker amplifier in order to produce sound (analog air pressure waves).

Working of D/A Converter

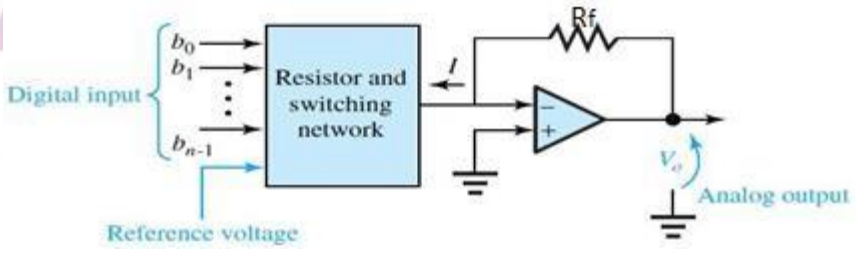


Fig.: Block diagram of DAC

- Fig. shows the block diagram of a typical digital-to-analog (D/A) converter, which accepts an *n*-bit parallel digital code as an input and provides an analog current or voltage as an output.
- For an ideal D/A converter, the analog output for an *n*-bit binary code is given by;
- $\mathbf{V_o = V_{ref}\,(-R_f/R)\,(b_0 + b_1 \times 2^{-1} + b_2 \times 2^{-2} + \cdots + b_{n-1} \times 2^{-n+1})}$

Where;

V_0 - Analog output voltage

V_{ref} - Reference analog input voltage

b_0 - Most significant bit of binary input code

b_{n-1} - Least significant bit of binary input code

- In order to provide current-to-voltage conversion and/or buffering, an op amp is used at the output. However, in some high-speed applications where a limited output voltage range is acceptable, a resistor, instead of an op amp, is used for the current-to-voltage conversion, thereby eliminating the delay associated with the op amp.

D/A Converter Specifications/Performance Parameters

Resolution

- The resolution of a D/A converter is the number of states (2^n) into which the full-scale range is divided or resolved. Here, n is the number of bits in the input digital word. The higher the number of bits, the better is the resolution.

$$Resolution = \frac{V_{ref}}{2^n - 1}$$

- The resolution in millivolts for the two cases for a full-scale output of 5 V is approximately20 mV (for an eight-bit converter) and 1.2 mV (for a 12-bit converter).

Accuracy

- The accuracy of a D/A converter is the difference between the actual analog output and the ideal expected output when a given digital input is applied.
- Sources of error include the gain error (or full-scale error), the offset error (or zero-scale error), nonlinearity errors and a drift of all these factors.

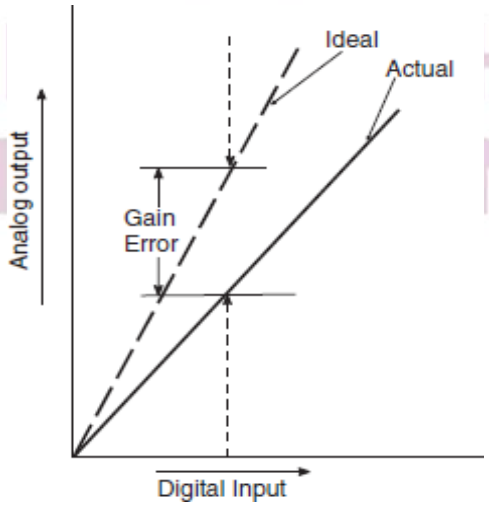


Fig.: Gain Error

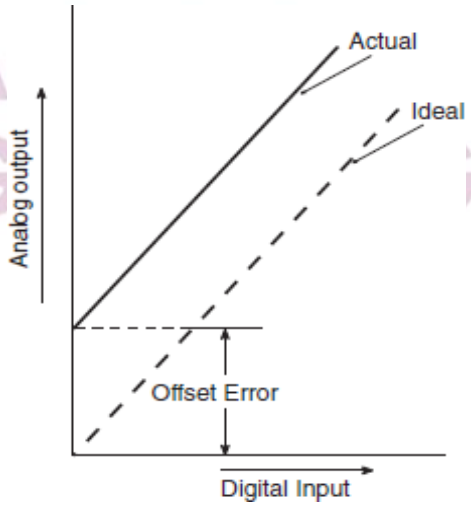


Fig.: Offset Error

Settling Time or Conversion Speed

- The conversion speed of a D/A converter is expressed in terms of its settling time.
- The *settling time* is the time period that has elapsed for the analog output to reach its final value within a specified error band after a digital input code change has been effected.
- General-purpose D/A converters have a settling time of several microseconds, while some of the high-speed D/A converters have a settling time of a few nanoseconds.

Dynamic Range

- This is the ratio of the largest output to the smallest output, excluding zero, expressed in dB.

Non Linearity or Differential Non Linearity

- **Nonlinearity (NL)** is the maximum deviation of analog output voltage from a straight line drawn between the end points, expressed as a percentage of the full-scale range or in termsof LSBs.
- **Differential non linearity (DNL)** is the worst-case deviation of any adjacent analog outputsfrom the ideal one-LSB step size.

Monotonocity

- A D/A converter is considered as monotonic if its analog output either increases or remains the same but does not decrease as the digital input code advances in one-LSB steps.

Types of D/A Converter

Binary Weighted Resistor D/A Converter

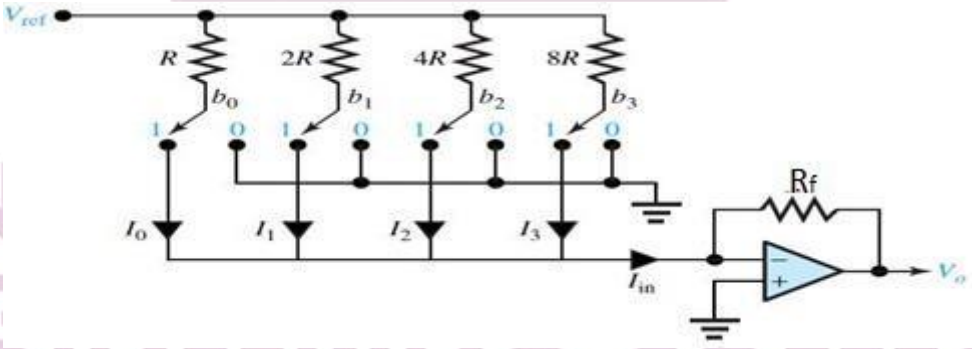


Fig.: 4 bit binary weighted resistor DAC

- Fig. shows a 4-bit weighted-resistor D/A converter which includes a reference voltage source, a set of four electronically controlled switches, a set of four binary-weighted precision resistors, and an Op-Amp.
- Each binary bit of digital input code controls its own switch. The switch closes with a bit value of1, and the switch stays open with binary 0. The resistor connected to the most significant bit (MSB), b_0, has a value of R; b_1 is connected to $2R$, b_2 to $4R$, and b_3 to $8R$.

- Thus, each low-order bit is connected to a resistor that is higher by a factor of 2. For a 4-bit D/A converter, the binary input range is from 0000 to 1111.
- The analog output voltage can be shown to be;

$$V_{out} = \frac{-V_{ref} R_f}{2^n R}(2^{n-1} b_{n-1} + 2^{n-2} b_{n-2} + ...+ 2b_1 + b_0)$$

- **Advantages**
  :
  1. Simple in Construction.
  2. Fast conversion.

- **Disadvantage:**
  1. The range of resistor values becomes impractical for binary words longer than 4 bits.
  2. The dynamic range of the Op-Amp limits the selection of resistance values.
  3. Expensive.

R – 2R Ladder D/A Converter

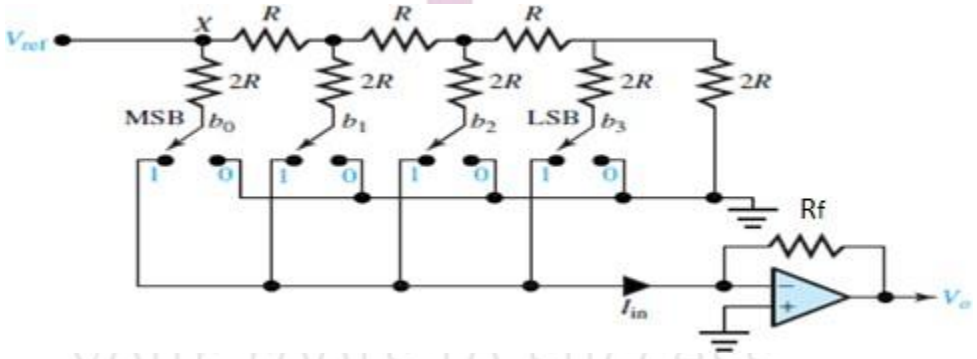


Fig.: 4 bit R – 2R Ladder DAC

- Fig. shows a 4-bit *R*–2*R* ladder D/A converter, which contains a reference voltage source, a set of four switches, two resistors per bit, and an op amp.
- The analog output voltage can be shown to be;

$$\mathbf{V_o = V_{ref}(-R_f/R)(b_0 \times 2^{-1} + b_1 \times 2^{-2} + \cdots + b_{n-1} \times 2^{-n})}$$

- **Advantages:**
  1. Because only two resistor values (*R* and 2*R*) are used, the *R*–2*R* ladder converter networks are relatively simple to manufacture
  2. Low cost.
  3. Practical and reliable.

- **Disadvantage:**
  1. More precise resistors required
  2. Slower conversion rate compare to weighted resistor DAC.

2^n – R D/A Converter

- An *n*-bit 2^n –*R* D/A converter needs 2^n resistors of equal value *R* and $(2^{n+1} - 2)$ analog switches.
- A 3-bit 2^n −*R* D/A converter is shown in Fig., which includes the eight resistors connected in series to form a voltage divider providing eight analog voltage levels, as well as 14 analog switches controlled by the digital input code such that each code creates a single path from the voltage divider to the converter output.

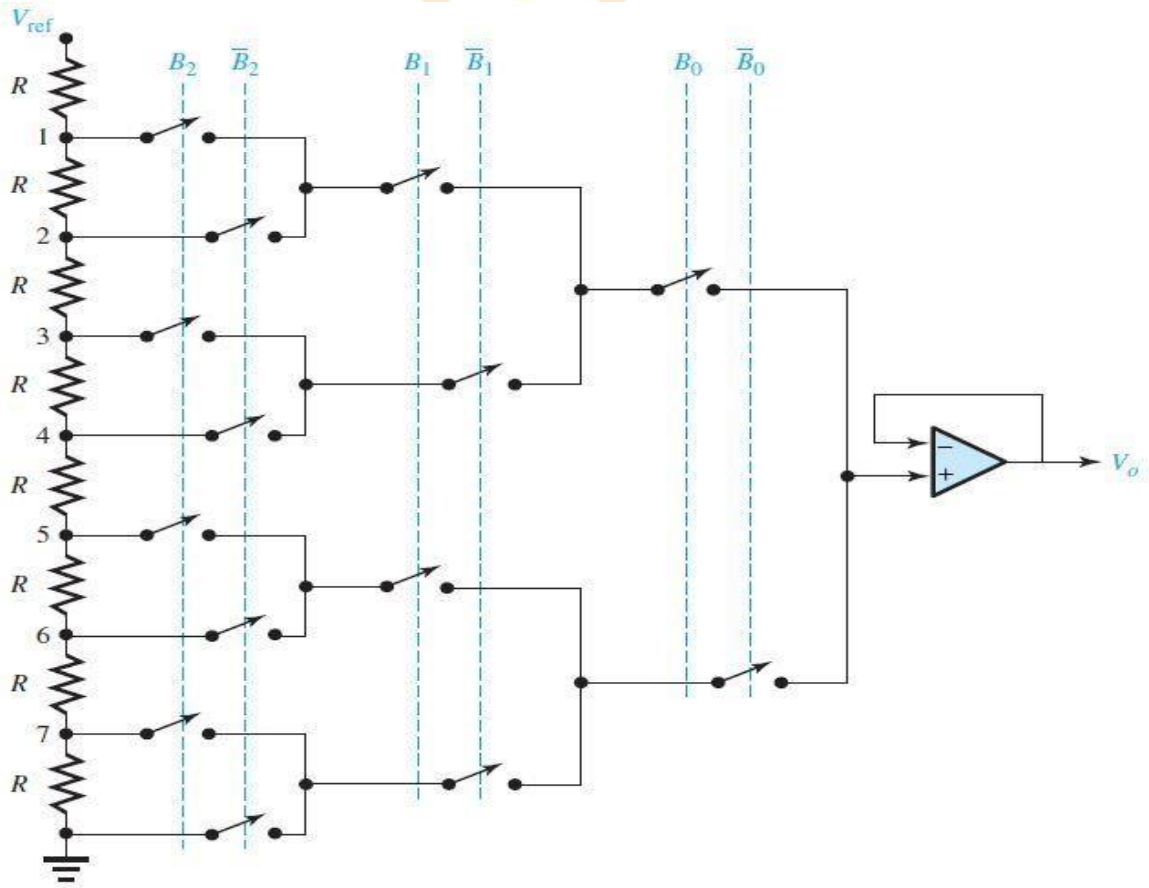


Fig.: 3 bit 2^n – *R* D/A converter

- A unit-gain amplifier is connected to the output in order to prevent loading of the voltage divider.
- **Advantages:**
  1. Because only single resistor values (*R*) are used, the 2^n – *R* converter networks are relativelysimple to manufacture
  2. Practical and reliable.

- **Disadvantage:**
  1. 2^n − *R* D/A converters are economically manufactured as LSI packages in spite of the large number of components needed.

Comparison of D/A Converter

Parameters	Weighted Resistor	R – 2R	2^n – R
Conversion time	Fast	Moderate	More
Accuracy	Less	Moderate	More
Construction	Simple	Very simple	Complex
Cost	Moderate	Less	More
Reliability	Less	More	Moderate

Mode of Operation for D/A Converter

Current Steering Mode of Operation

- In the *current steering mode* of operation of a D/A converter, the analog output is a current equalto the product of a reference voltage and a fractional binary value D of the input digital word. Where,

$$D = \frac{2^n - 1}{2^n}$$

- E.g. For R – 2R DAC analog output voltage $= -\left(\frac{2^n-1}{2^n}\right) V_{ref}$

Voltage Switching Mode of Operation

- In the *voltage switching mode* of operation of R - 2R ladder type D/A converter, the reference voltage is applied to the inverting terminal of op amp and the output is taken from the reference voltage terminal. Non inverting terminal of op amp is joined to analog ground.

- E.g. For R – 2R DAC analog output voltage $= -V_{ref}\ (-R_f/R)\ (b_0 \times 2^{-1} + b_1 \times 2^{-2} + \cdots + b_{n-1} \times 2^{-n})$

BCD Input D/A Converter

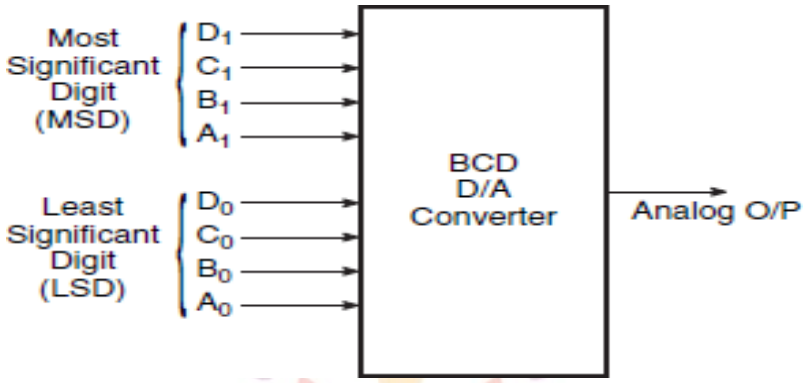


Fig. BCD input D/A converter

- A BCD-input D/A converter accepts the BCD equivalent of decimal digits at its input. A two-digit BCD D/A converter for instance is an eight-bit D/A converter.
- Fig. shows the circuit representation of an eight-bit BCD-type D/A converter. Such a converter has 99 steps and accepts decimal digits 00 to 99 at its input. A 12-bit converter will have 999 steps.
- The weight of the different bits in the least significant digit (LSD) will be 1 (for A_0), 2 (for B_0), 4 (for C_0) and 8 (for D_0).
- The weights of the corresponding bits in the next higher digit will be 10 times the weights of corresponding bits in the lower adjacent digit.
- For the D/A converter shown in Fig. the weight of the different bits in the most significant digit (MSD) will be 10 (for A_1), 20 (for B_1), 40 (for C_1) and 80 (for D_1).
- In general, an n-bit D/A converter of the BCD input type will have $(10^{n/4} - 1)$ steps.
- The percentage resolution of such a converter is given by $[1/(10^{n/4} - 1)]\times 100$.

Integrated Circuit (IC) D/A Converter

DAC – 08

- DAC-08 is an eight-bit monolithic D/A converter.

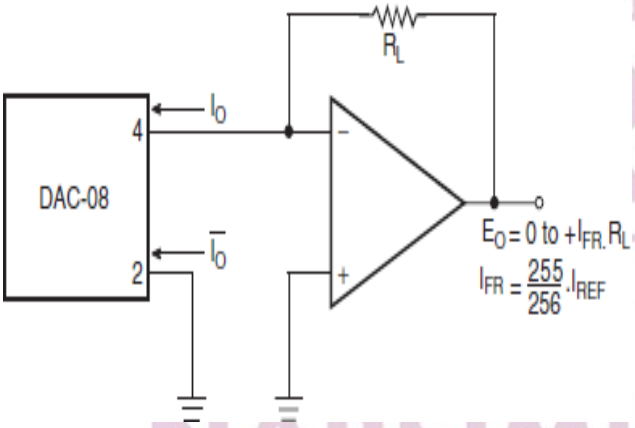


Fig.: DAC-08 for positive output operation

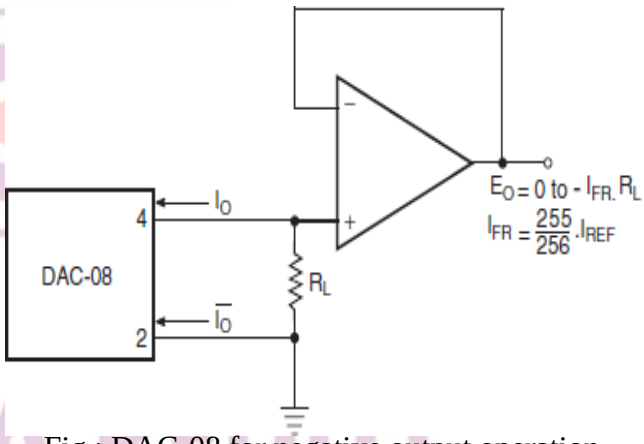


Fig.: DAC-08 for negative output operation

- **Advantages:**
  1. Less settling time
  2. High voltage compliance
  3. Wide power supply range
  4. High linearity

- **Applications:**
  - Waveform generators, servomotor driver, audio encoders and attenuators, analog meter drivers, programmable power supplies, high-speed modems, CRT display drivers, etc.

7.8.2 DAC – 0808

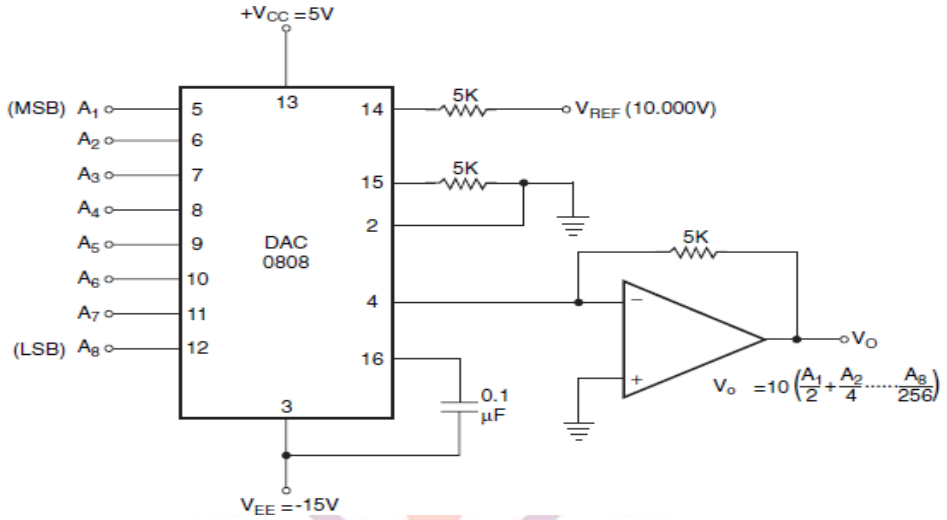


Fig.: DAC 0808 wired as a voltage-output D/A converter

- **Advantages:**
  1. Less settling time
  2. More accuracy
  3. Wide power supply range
  4. High linearity
  5. Direct interface with TTL, CMOS logic families

- **Applications:**
  - Voltage output DAC

DAC AD-7524

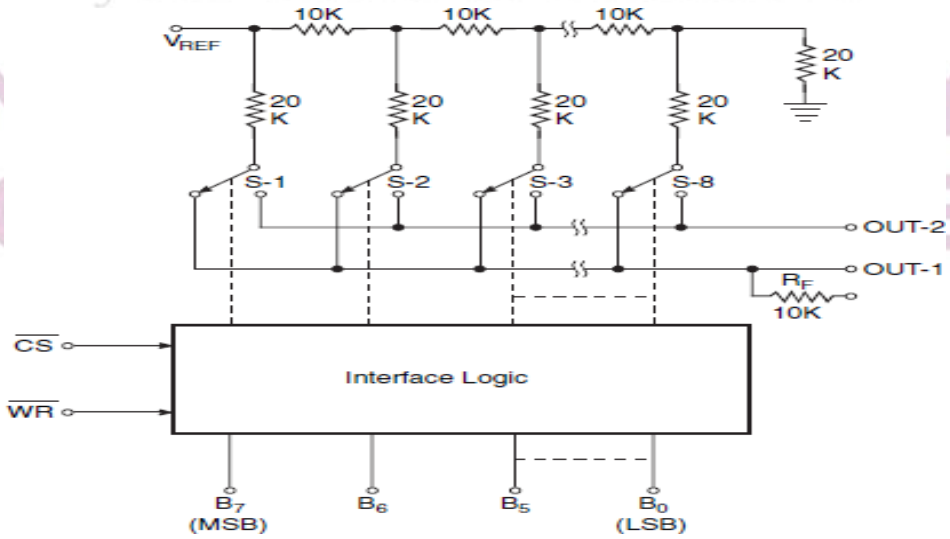


Fig.: Functional diagram of AD 7524

- **Advantages:**
  1. Direct interface with many microprocessor
  2. Less power dissipation
  3. Monotonocity
  4. High linearity
  5. Wide power supply range

- **Applications:**
  - Microprocessor-controlled gain setting and signal control applications.

D/A Converter Applications

1. DAC as multiplier
2. DAC as divider
3. In programmable integrator
4. In low frequency function generator
5. In digitally controlled filter etc.

D/A Converter Examples

1. An eight-bit D/A converter has a step size of 20 mV. Determine the full-scale output andpercentage resolution.

Sol.:

- $[1/(2^8 -1)]\times V = 20 \times 10^{-3}$, where V is the voltage corresponding to a logic '1'.
- This gives $V = 20 \times 10^{-3} \times (2^8 - 1) = 5.1$ V.
- The full-scale output = $[(2^n - 1)/2^n] \times V = [(2^8 - 1)/2^8] \times 5.12 = (255/256) \times 5.12 = 5.1$V.
- The percentage resolution = $[1/(2^n - 1)] \times 100 = 100/255 = 0.392\%$.
- The percentage resolution can also be determined from:

  (Step size/full-scale output) × 100 = $(20 \times 10^{-3}/5.1) \times 100 = 0.392$ %

2. A certain eight-bit D/A converter has a full-scale output of 5 mA and a full-scale error of ±0.25% of full scale. Determine the range of expected analogue output for a digital input of 10000010.

Sol.:

- $\text{Step size} = \dfrac{\text{Full-scale output}}{\text{Number of steps}}$

$$= \frac{5 \times 10^{-3}}{2^8 - 1}$$

$$= 19.6\ \mu\text{A}$$

- For a digital input of 10000010 ($= 130_{10}$) the analogue output is given by $130 \times 19.6 = 2.548$ mA.
- $\text{Error} = \pm\dfrac{0.25 \times 5 \times 10^{-3}}{100}$

$$= \pm 12.5\ \mu\text{A}$$

- The expected analogue output will therefore be in the range 2.5355–2.5605 mA.

Analog to Digital Converter (A/D Converter)

- The A/D converter converts analog input signals into digital output data in many areas such process control, aircraft control, and telemetry. Being the interface between analog systems and digital systems, it plays a key role in many industrial, commercial, and military systems.
- Several types of A/D converters exist: counter-controlled, successive-approximation, flash (parallel comparators) and dual-ramp (dual-slope) converters.
- The commercially available LM311 is an example that is widely used by designers.

A/D Converter Specifications/Performance Parameters

Resolution

- Resolution is ration of a change in input voltage needed to change the digital output by 1 LSB.

$$Resolution = \frac{V_{in}}{2^n - 1} \; ; n = no.of\ bits$$

Accuracy

- The accuracy specification describes the maximum sum of all errors, both from analog sources and from the digital sources of the A/D converter.

Gain and Offset Error

- The ***gain error*** is the difference between the actual full-scale transition voltage and the ideal full-scale transition voltage.
- The ***offset error*** is the error at analogue zero for an A/D converter operating in bipolar mode.

Gain and Offset Drift

- The ***gain drift*** **is** the change in the full-scale transition voltage measured over the entire operating temperature range.
- The ***offset drift*** is the change with temperature in the analogue zero for an A/D converter operating in bipolar mode.

Sampling Frequency and Aliasing Phenomenon

- According sampling theorem, the minimum rate at which the analog signal should sampled twice the highest frequency in the analog signal.

$$f_s \geq 2f_{max} \qquad (Nyquist\ criterion)$$

- If Nyquist criterion is not fulfilled then overlapping of signals is occur it is known as aliasing.

Quantization Error

- The difference between an input value and its quantized value (such as round-off error) is referred to as quantization error.

Non Linearity and Differential Non Linearity

- **Non linearity** is measure of the maximum deviation of actual ADC transfer function from straight line drawn through the first and last code transition after correction for offset and gain error.
- **Differential non linearity** is measure of the maximum of difference in the each conversion's Current Code Width (CCW) and the Ideal Code Width (ICW).

Conversion Time

- Total time required to convert an analog signal in to digital output.

Aperture and Acquisition Time

- ***Acquisition time*** is the time required for the electronic switch to close and the hold capacitorto charge
- ***Aperture time*** is the time needed for the switch completely to open after the occurrence of the hold signal.

7.10.10 Code Width

- The *code width* is the quantum of input voltage change that occurs between the output codes transitions expressed in LSBs of full scale.

Types of A/D Converter

Counter Controlled A/D Converter

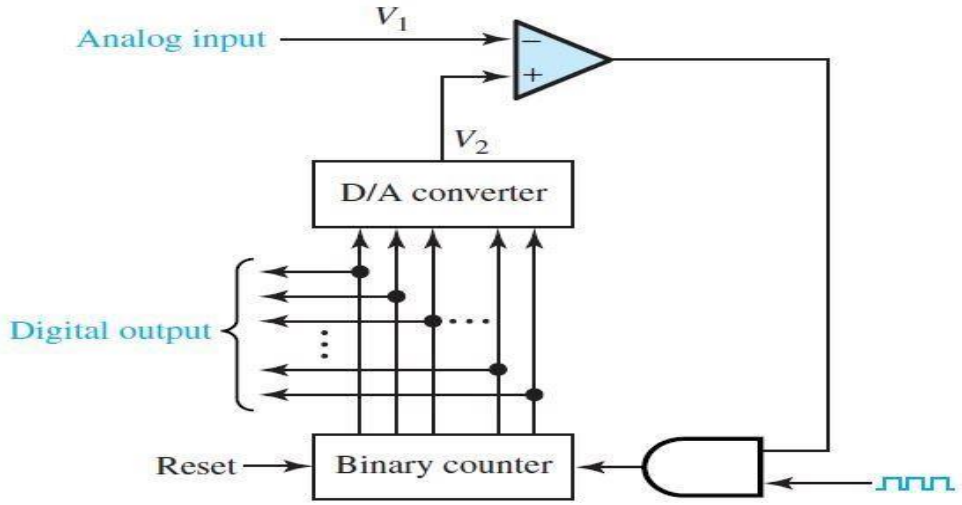


Fig.: counter-controlled A/D converter

- Resetting the binary counter to zero produces D/A output voltage $V_2 = 0$ and initiates the analog-to-digital conversion.
- When the analog input V_1 is larger than the DAC (D/A converter) output voltage, the comparator output will be high, thereby enabling the AND gate and incrementing the counter.
- V_2 is increased as the counter gets incremented; when V_2 is slightly greater than the analog input signal, the comparator signal becomes low, thereby causing the AND gate to stop the counter. The counter output at this point becomes the digital representation of the analog input signal.
- The relatively long conversion time needed to encode the analog input signal is the major disadvantage of this method.

Successive Approximation A/D Converter

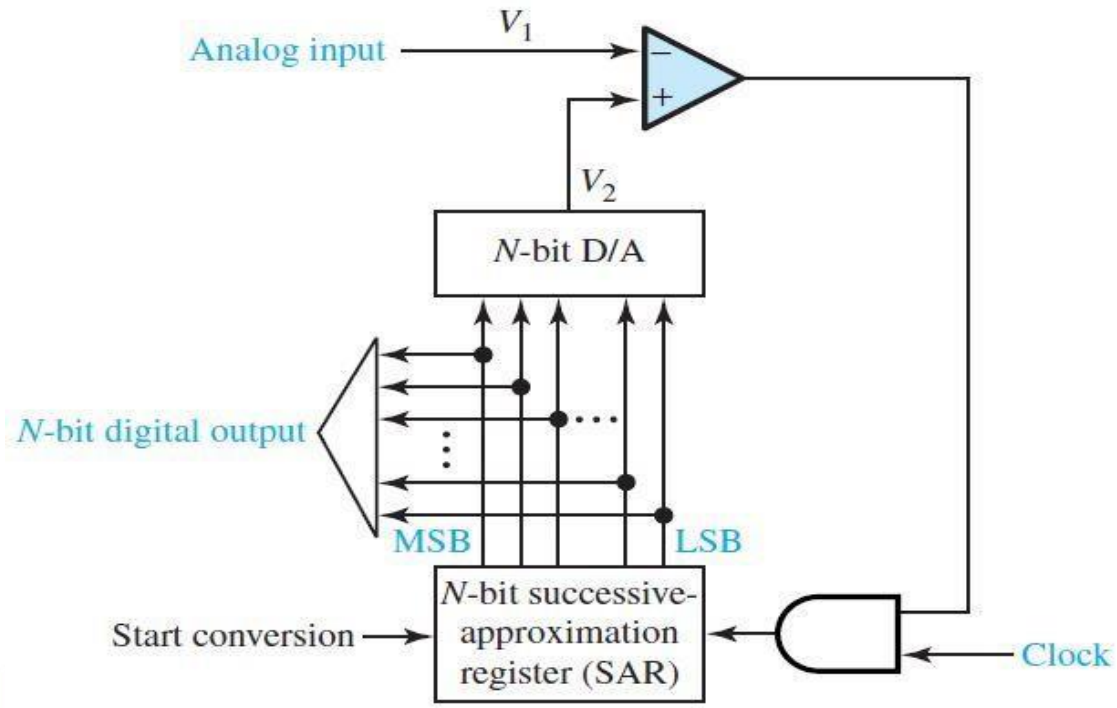


Fig.: Successive Approximation A/D converter

- This converter, shown in Fig., also contains a D/A converter, but the binary counter is replaced by a successive-approximation register (SAR), which makes the analog-to-digital conversion much faster.
- On the other hand, if the signal to be converted is larger than the D/A computer output, then the MSB remains 1. This procedure is repeated for each bit until the binary equivalent of the input analog signal is obtained at the end.
- This method requires only n clock periods, compared to the 2n clock periods needed by the counter-controlled A/D converter, where n is the number of bits required to encode the analog signal.

Dual Ramp or Dual Slop A/D Converter

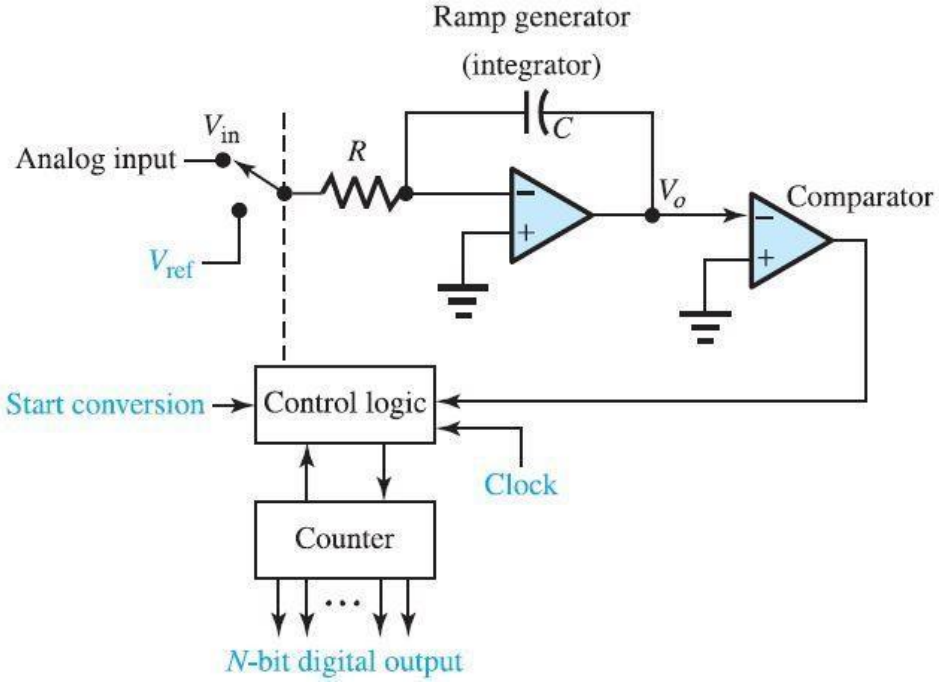


Fig.: Dual Ramp A/D converter

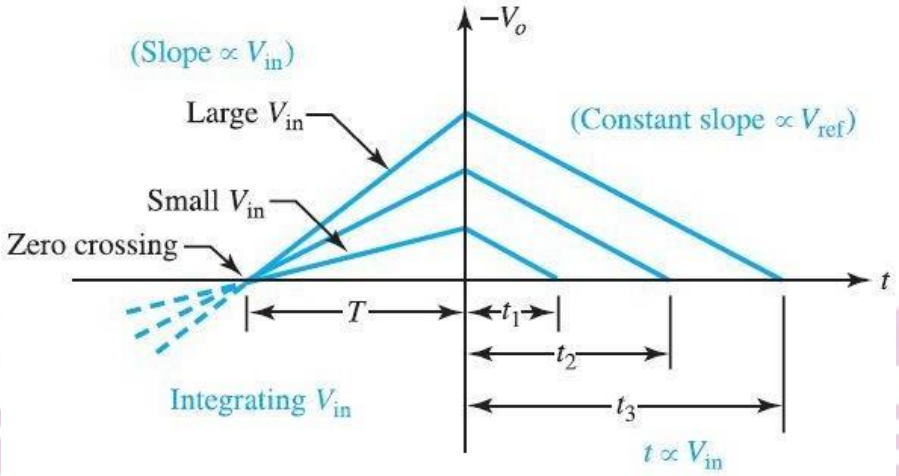


Fig.: Output of ramp generator in dual-ramp A/D converter

- After a start-of-conversion pulse, the counter is cleared and the analog input V_{in} becomes the input of the ramp generator (integrator). When the output of the ramp generator V_o reaches zero, the counter starts to count.
- After a fixed amount of time T, as shown in Fig., the output of the ramp generator is proportional to the analog input signal. At the end of T, the reference voltage V_{ref} is selected, when the integrator gives out a ramp with a positive slope.

- As V_o increases, the counter is incremented until Vo reaches the comparator threshold voltage of 0 V, when the counter stops being incremented again.
- The value of the counter becomes the binary code for the analog voltage V_{in}, since the number of clock pulses passing through the control logic gate for a time t is proportional to the analog signal Vin.
- Dual-ramp A/D converters can provide accuracy at low cost, even though the process is slow because a double clock pulse count is an inherent part of the process.

Flash Type A/D Converter

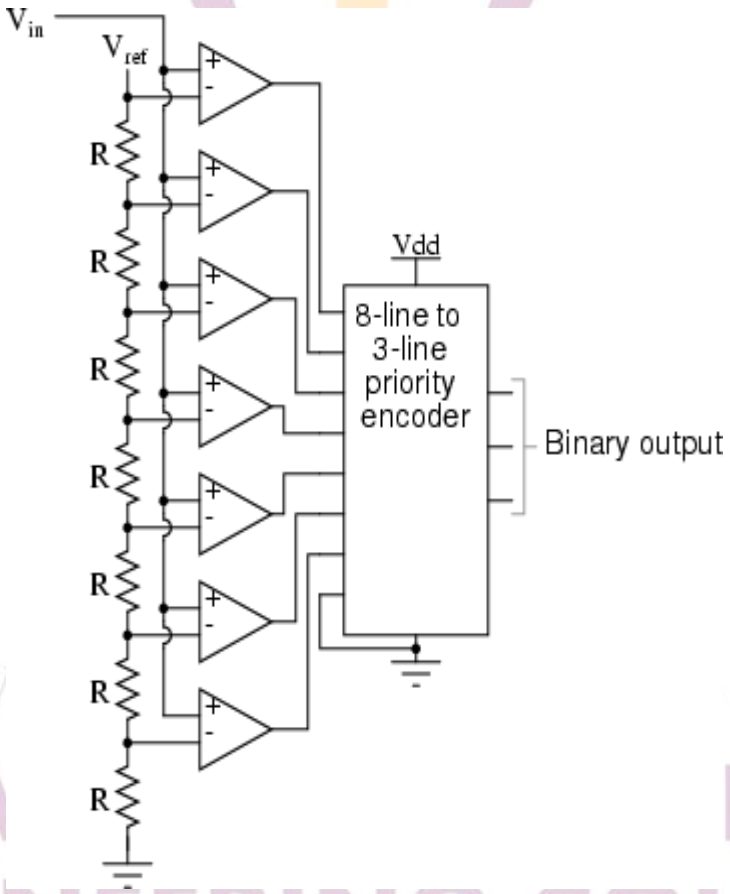


Fig.: 3 bit flash type ADC

- Flash Type ADC is based on the principle of comparing analog input voltage with a set of reference voltages.
- To convert the analog input voltage into a digital signal of n-bit output, $(2^n - 1)$ comparators are required.
- The seven $(2^n - 1)$ op-amps are used as comparators. The non-inverting inputs of all the seven comparators are connected to the analog input voltage. The inverting terminals are connected to a set of resistive divider network and power supply +V.

- The output of the comparator is in positive saturation (i.e. logic 1), when voltage at non-inverting terminal is greater than voltage at inverting terminal and is in negative saturation otherwise.
- A Priority Encoder is used to transform the comparator outputs to the correct digital binary output.

- **Advantages:**
  1. It is the fastest type.
  2. Typical conversion time is 100ns or less.
  3. The construction is simple and easier to design.

- **Disadvantages:**
  1. It is not suitable for higher number of bits.
  2. To convert the analog input voltage into a digital signal of n-bit output, $(2^n - 1)$ comparators are required. The number of comparators required doubles for each added bit.

Integrated A/D Converters

7.14.1 ADC 0800

- ADC-0800 is a successive approximation type eight-bit A/D converter. The basic architecture of ADC-0800 is shown in Fig.

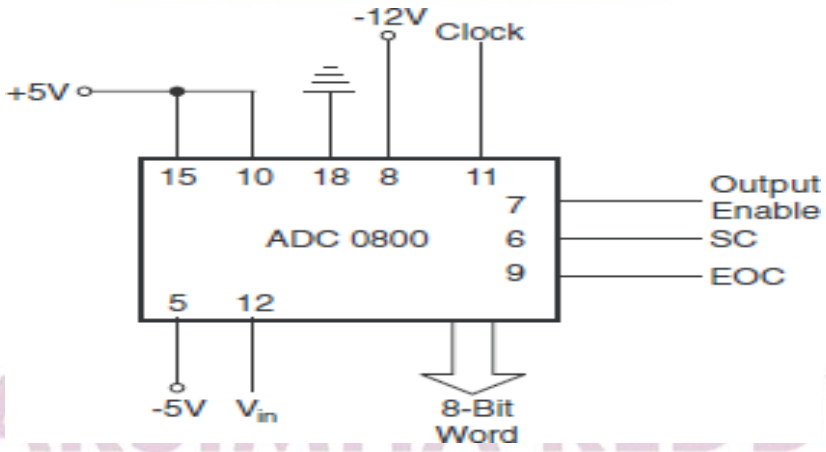


Fig.: ADC 0800

7.14.2 ADC 0808

- ADC 0808 is an eight-bit CMOS successive approximation type A/D converter. The device has aneight-channel multiplexer and a microprocessor-compatible control logic.
- Salient features of the device include eight-bit resolution, no missing codes, a conversion time of 100 s (typical), stand-alone operation or easy interface to all microprocessors, a 0 - 5 V analogue input range with a single 5 V supply and latched tristate outputs. Fig. shows the internal architecture of the device.

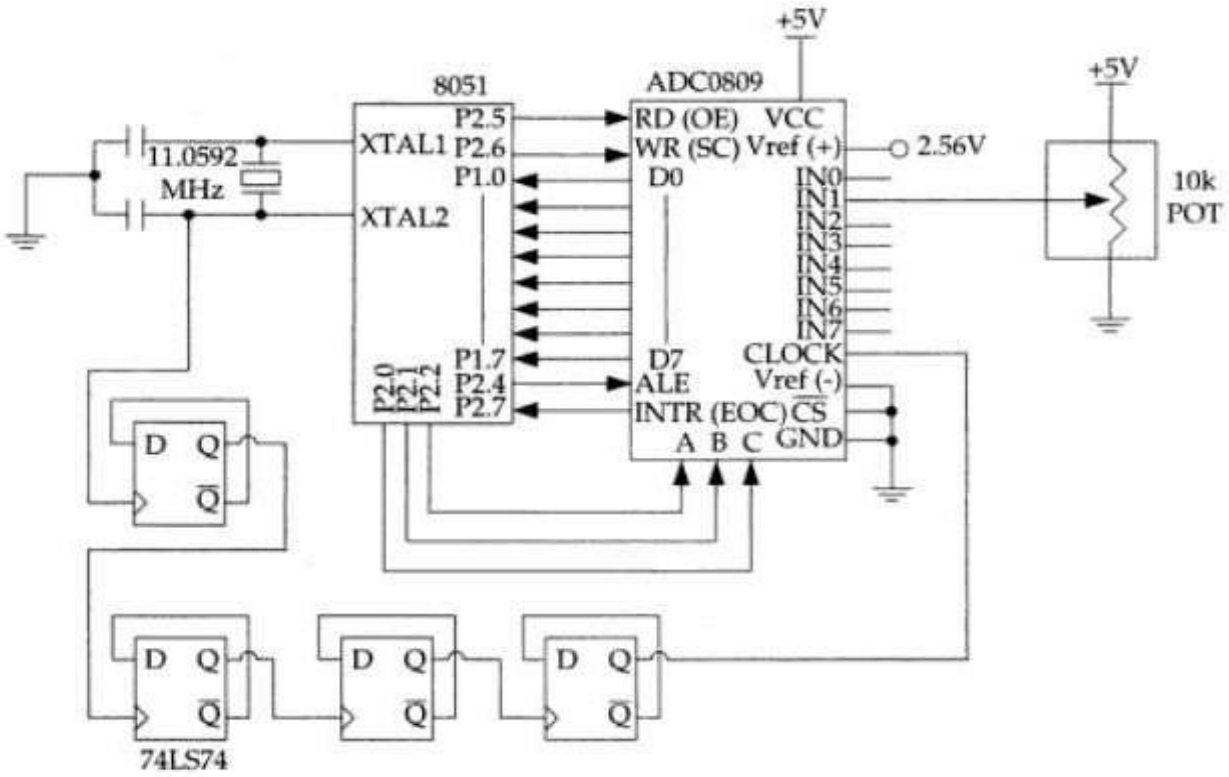


Fig.: Interfacing of ADC 0808

Comparison of A/D Converter

Parameters	Flash Type ADC	Successive Approximation ADC	Dual Slop ADC
Speed	Fastest	Fast	Slow
Accuracy	Less	Medium	More
Resolution	Up to 2^8	Up to 2^{16}	2^{16} or more
Input hold time	Very less	More than Flash type	More
Cost	Very costly	Medium	Less
Applications	Fiber optic comm.,DSO etc.	Data Acquisition	Where more accuracy is required

A/D Converter Applications

1. Data acquisition system
2. Communication system
3. Digital multimeter
4. Cell phone

5. CRO etc.

A/D Converter Examples

1. **Determine the resolution of a 12-bit A/D converter having a full-scale analogue input voltageof 5 V.**

Sol.:

- A 12-bit A/D converter resolves the analogue input voltage into $(2^{12} - 1)$ levels.
- The resolution $= 5/(2^{12} - 1) = 5000/(4096 - 1) = (5000/4095) = 1.22mV.$

2. **The data sheet of a certain eight-bit A/D converter lists the following specifications: resolutioneight bits; full-scale error 0.02% of full scale; full-scale analogue input +5 V. Determine (a) thequantization error (in volts) and (b) the total possible error (in volts).**

Sol.:

(a) The eight-bit A/D converter has $2^8 - 1 = 255$ steps. Therefore, the quantization error $= 5/255 = 5000/255 = 19.607$ mV.

(b) The full-scale error $= 0.02\% of full scale = 0.02 \times 5000/100 = 1$ mV. Therefore, the total possible error $= 19.607 + 1 = 20.607mV.$

Points to consider of selection for D/A & A/D Converter

1. Accuracy
2. Resolution
3. Dynamic specifications
4. Conversion speed
5. Analog and digital input signal
6. Environmental condition
7. Sampling mechanism
8. Error etc.